Cover Sheet and Revision Status				
版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20160004	Mar. 22, 2016	New issue	Hank Lin
2.0	20190016	Sep. 02, 2019	EOL 24L SSOP-150mil	Hank Lin

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■ Description

The CS8817, 16-channel constant current LED driver with double latch display technology, is suitable for any static and dynamic applications. The distinctive double latch technology enhances the visual refresh rate and low grayscale uniformity by increasing LED utilization rate. And the ghost image abatement is designed to eliminate ghosting of multiplexing LED modules due to parasitic capacitors.

The device operates over a 3.3V to 5V input voltage range (±10%) and provides 16 open-drain constant current sinking outputs that are rated to 17 V and delivers up to 45mA of high accuracy current to each string of LED. The current at each output is programmable by means of an external current-sensing resistor.

The CS8817's on-board pass elements minimize the need for external components, while at the same time, providing ±3% channel current accuracy and ±4% chip current accuracy. Additional features include a ±0.1% regulated output current capability.
The CS8817 is available in a 24L SSOP-236mil package and specified over the -40℃ to +85℃ ambient temperature range.

■ Feature

- 3.3V ~ 5.0V Operating supply voltage (±10%)
- 5~45mA/5V Constant current output range
- 5~30mA/3.3V Constant current output range
- 17V Rated output channels for long LED strings
- ±3% (max.) Current accuracy between channels
- ±4% (max.) Current accuracy between chips
- ±0.1% Output current regulation capability
- Double latch display technology (Patent approved)
- Visual refresh rate, LED utilization rate, grayscale level and low brightness uniformity are better than conventional pure drivers
- Current setting by one external resister
- Ghost image abatement
- High HBM ESD protection (Iout pin > 8000V)
- -40℃ to +85℃ Ambient temperature range

■ Product Family

CS8817AF ------- 24SSOP (236mil, 1.0mm lead-pitch)

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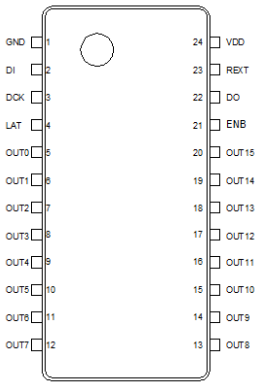
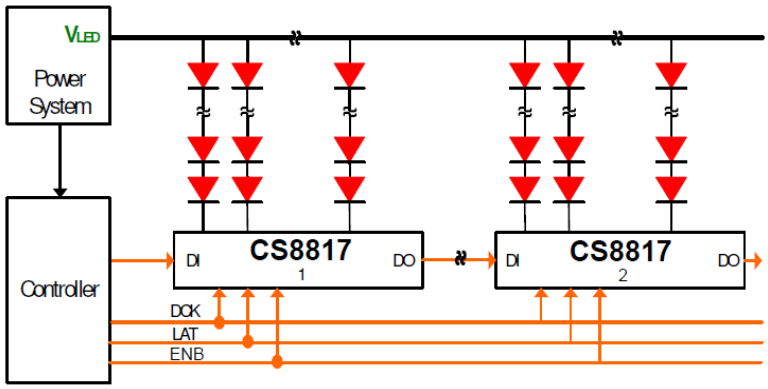
■ Pin Assignment



24L SSOP

■ Typical Operating Circuits



■ Pin Description

Pin No.	Pin Name	Function
1	GND	GND Pin.
2	DI	Serial input data pin.
3	DCK	Clock input terminal for shift register, rising edge trigger.
4	LAT	Input terminal of data strobe.
5~20	OUT0~OUT15	16 constant current output pin to drive common anode LEDs.
21	ENB	Data output enable pin, when ENABLE=High-level, all OUT0~OUT15 are turned off, and when ENABLE=Low-level, all OUT0~OUT15 are enabled.
22	DO	Serial data output pin for cascade operation.
23	REXT	The external resistor connection pin to adjust the output current.
24	VDD	3.3V~5.5V supply voltage pin.

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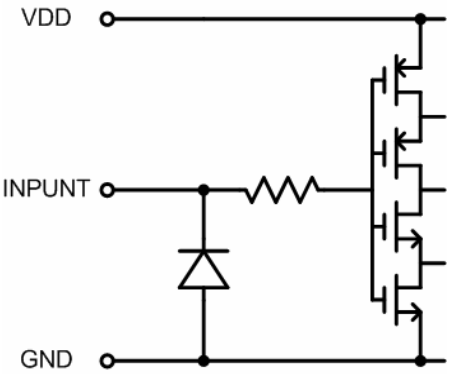
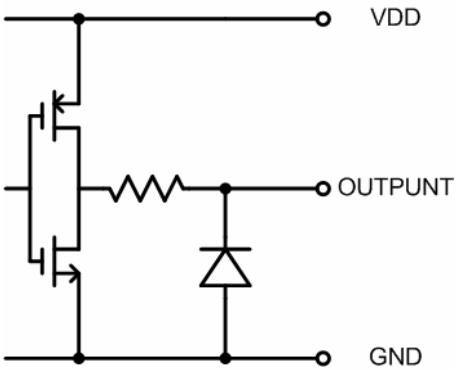
■ Equivalent Circuits of I/O Pins

DCK, DI, LAT, ENB terminals



DO terminal



■ Absolute Maximum Ratings *(Ta=25 °C, Tj(max) = 150 °C)*

Characteristics	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3~7.0	V
Input Voltage	VIN	-0.3 to VDD+0.3	V
Output Current	IOUT	45	mA
Output Voltage	VOUT	-0.3 to 17	V
GND Pin Current	IGND	800	mA
Clock Frequency	FDCK	30	MHz
Thermal Resistance (On PCB)	Rth(j-a)	24L SSOP-236mil : 57.7	℃/W
Operating Temperature	Top	-40 to 85	℃
Storage Temperature	Tstg	-55 to 150	℃

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.
(2) All voltage values are with respect to ground terminal.

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■ Electrical Characteristics *(VDD = 3.3 V, Ta = 25 °C unless otherwise noted)*

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 Ma	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel)	dIOUT1	VOUT = 1.0V Rrext = 0.94 KΩ	—	±1.0	±3.0	%
Output Current Skew (Chip-to-Chip)	dIOUT2		—	±1.0	±4.0	%
Output Current Skew (Channel-to-Channel)	dIOUT3	VOUT = 1.0 V Rrext = 6.4 KΩ	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)	dIOUT4			±1.5	±4.0	%
Output Voltage Regulation	% /VOUT	Rrext = 0.94 KΩ, VOUT = 1V ~ 3V	—	±0.1	—	% / V
Supply Voltage Regulation	% /VDD	Rrext = 0.94 KΩ, VDD = 3V ~ 5.5V	—	±0.7	±1	
Supply Current	$I_{DD1(off)}$	input signal is static Rrext = 3.69 KΩ all outputs turn off	—	1.6	—	mA
	$I_{DD2(on)}$	input signal is static Rrext = 3.69 KΩ all outputs turn on	—	2.5	—	
	$I_{DD3(off)}$	input signal is static Rrext = 0.94 KΩ all outputs turn off	—	4.5	—	
	$I_{DD4(on)}$	input signal is static Rrext = 0.94 KΩ all outputs turn on	—	5.5	—	

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■ Electrical Characteristics *(VDD = 5.0 V, Ta = 25 °C unless otherwise noted)*

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 1 mA	—	—	0.4	V
	VOH	IOH= 1 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel)	dIOUT1	VOUT = 1.0 V Rrext = 0.94 KΩ	—	±1.0	±3.0	%
Output Current Skew (Chip-to-Chip)	dIOUT2		—	±1.0	±3.0	%
Output Current Skew (Channel-to-Channel)	dIOUT3	VOUT = 1.0 V Rrext = 3.69 KΩ	—	±1.5	±3.0	%
Output Current Skew (Chip-to-Chip)	dIOUT4			±1.5	±4.0	%
Output Voltage Regulation	% /VOUT	Rrext = 0.94 KΩ, VOUT = 1 V ~ 3 V	—	±0.1	—	% / V
Supply Voltage Regulation	% /VDD	Rrext = 0.94 KΩ, VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current	$I_{DD1(off)}$	input signal is static Rrext = 3.69 KΩ all outputs turn off	—	1.6	—	mA
	$I_{DD2(on)}$	input signal is static Rrext = 3.69 KΩ all outputs turn on	—	2.5	—	
	$I_{DD3(off)}$	input signal is static Rrext = 0.94 KΩ all outputs turn off	—	4.5	—	
	$I_{DD4(on)}$	input signal is static Rrext = 0.94 KΩ all outputs turn on	—	5.5	—	

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■ Switching Characteristics *(VDD = 3.3 V, Ta = 25 °C unless otherwise noted)*

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L‘ to ‘H’)	ENB-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 1820 Ω □ VL =5.0 V RL = 330 Ω □ CL = 13 pF	—	—	—	ns
	DCK-to-DO	tpLH3		—	35	—	
Propagation Delay (‘H’ to ‘L’)	ENB-to-OUT0	tpHL1		—	—	—	
	DCK-DO	tpHL3		—	35	—	
Pulse Duration	ENB	$tw_{(ENB)}$		120	—	—	
	LAT	$tw_{(LAT)}$		20	—	—	
	DCK	$tw_{(DCK)}$		15	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		5	—	—	
	DI	$tsu_{(DI)}$		3	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(DI)}$		4	—	—	
DO Rise Time		$tr_{(DO)}$		—	20	—	
DO Fall Time		$tf_{(DO)}$		—	20	—	
Output Voltage Rise Time (turn-off)		tor		—	55	—	
Output Voltage Fall Time (turn-on)		tof		—	50	—	

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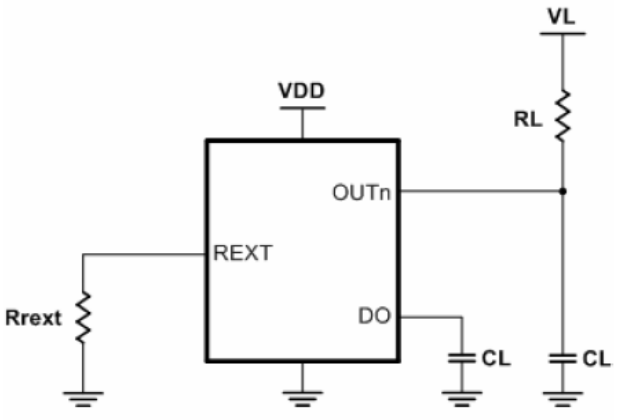
■ Switching Characteristics *(VDD = 5.0 V, Ta = 25 °C unless otherwise noted)*

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay (‘L‘ to ‘H’)	ENB-to-OUT0	tpLH1	VIH = VDD VIL = GND Rrext = 1820 Ω VL =5.0 V RL = 330 Ω□ CL = 13 pF	—	—	—	ns
	DCK-to-DO	tpLH3		—	24	—	
Propagation Delay (‘H’ to ‘L’)	ENB-to-OUT0	tpHL1		—	—	—	
	DCK-DO	tpHL3		—	24	—	
Pulse Duration	ENB	$tw_{(ENB)}$		80	—	—	
	LAT	$tw_{(LAT)}$		20	—	—	
	DCK	$tw_{(DCK)}$		15	—	—	
Setup Time	LAT	$tsu_{(LAT)}$		5	—	—	
	DI	$tsu_{(DI)}$		3	—	—	
Hold Time	LAT	$th_{(LAT)}$		20	—	—	
	DI	$th_{(DI)}$		4	—	—	
DO Rise Time		$tr_{(DO)}$		—	15	—	
DO Fall Time		$tf_{(DO)}$		—	15	—	
Output Voltage Rise Time (turn-off)		tor		—	35	—	
Output Voltage Fall Time (turn-on)		tof		—	35	—	



Switching Characteristics Test Circuit

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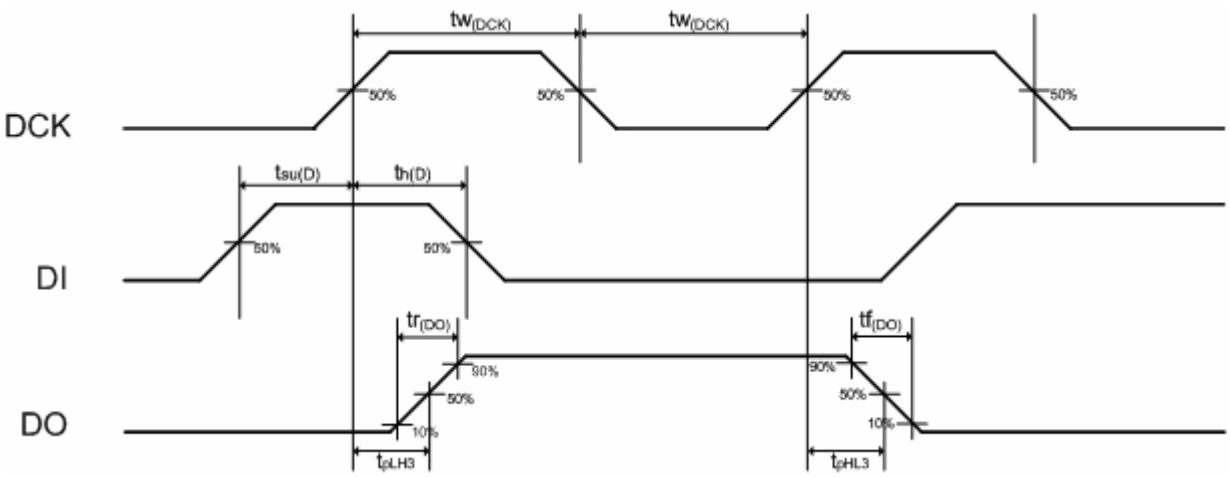
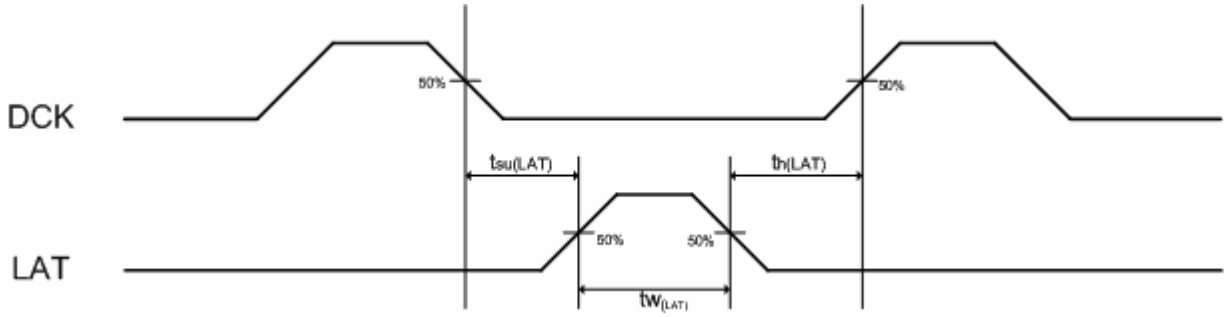
■ Timing Waveform

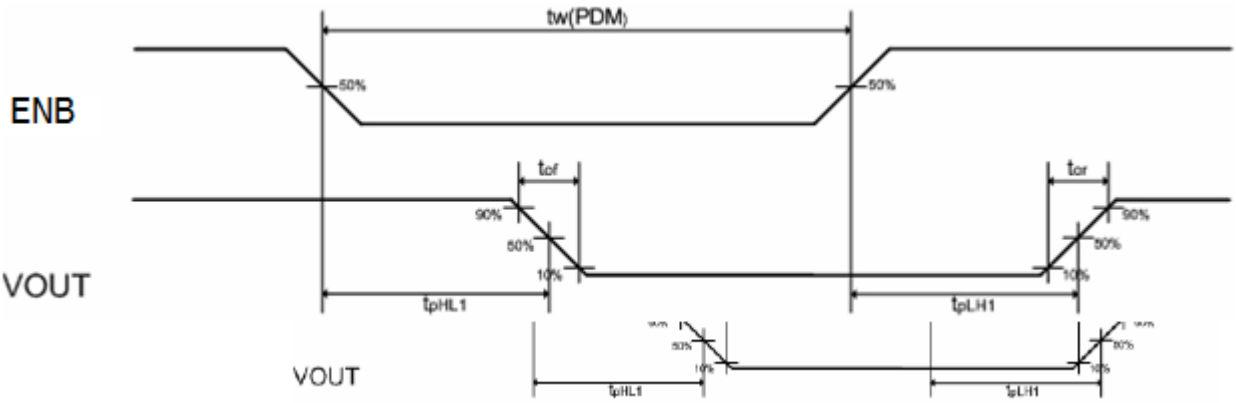
DCK-DI, DO



DCK-LAT



ENB-VOUT



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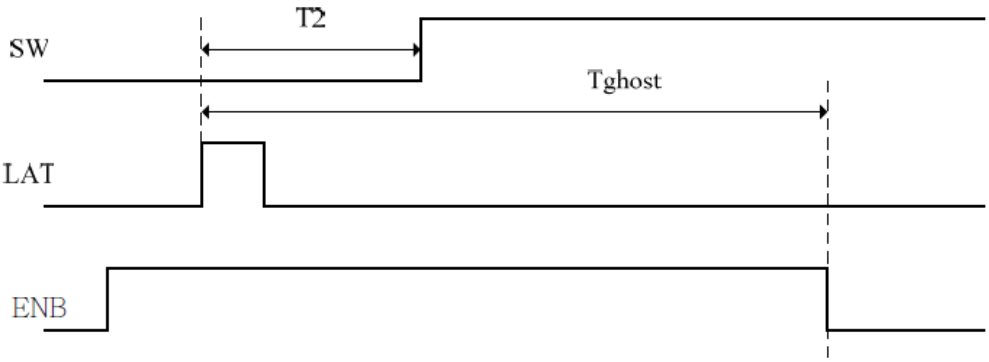
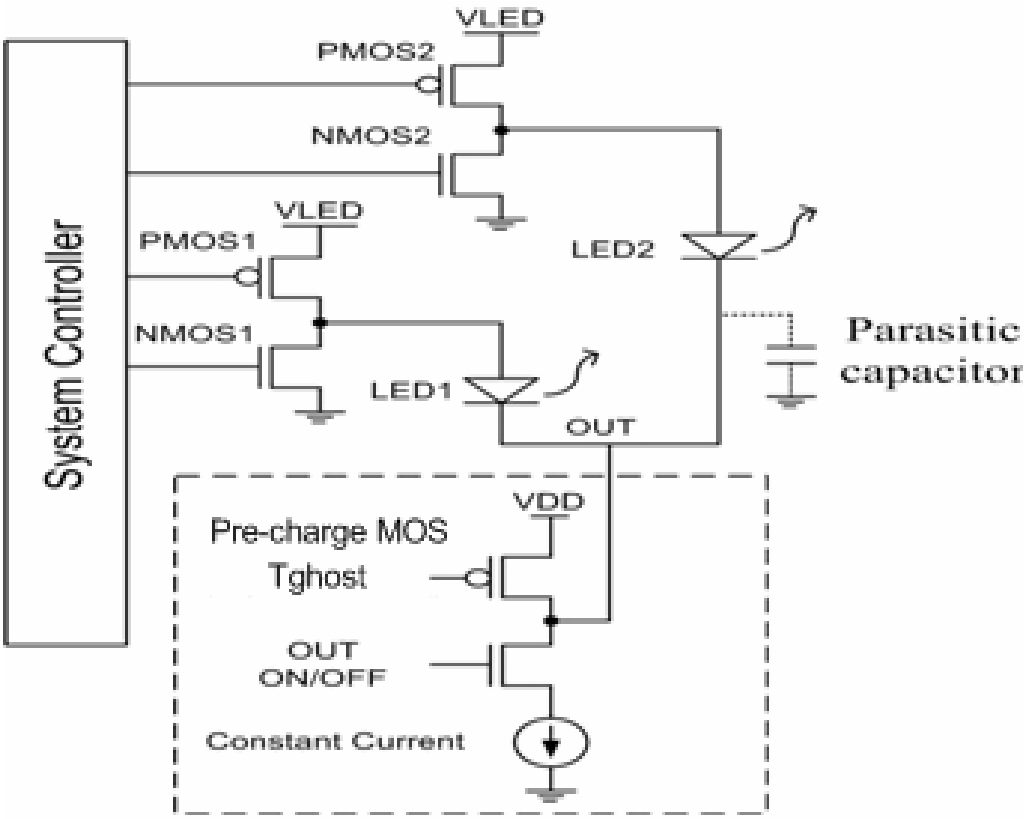
Ghost Image Abatement

CS8817 provides internal pre-charge circuit to reduce ghost phenomenon of multiplexing display due to parasitic capacitors. When ENB=high, the voltage of output channels will be pulled high from the rising edge of LAT signal to the falling edge of ENB signal (Tghost), so the reverse bias would only happened in Tghost. Such design can prevent LED damage due to the reverse bias for long time. In Tghost, the high voltage on the parasitic capacitor prevents the inrush current resulting from turning on the switching PMOS of next scan line. (It is recommended to let Tghost ≧ 2000ns, where SW signal is the multiplexing switch signal.)





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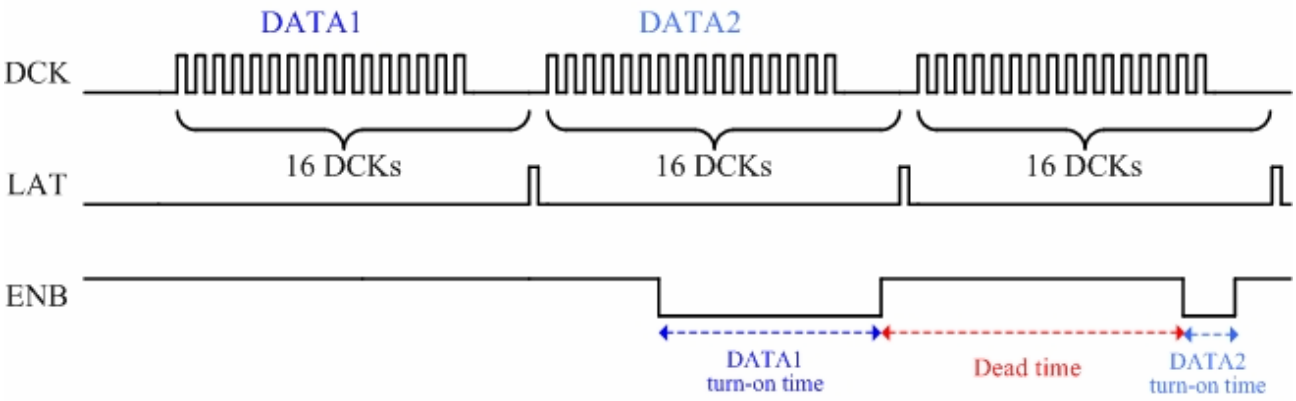
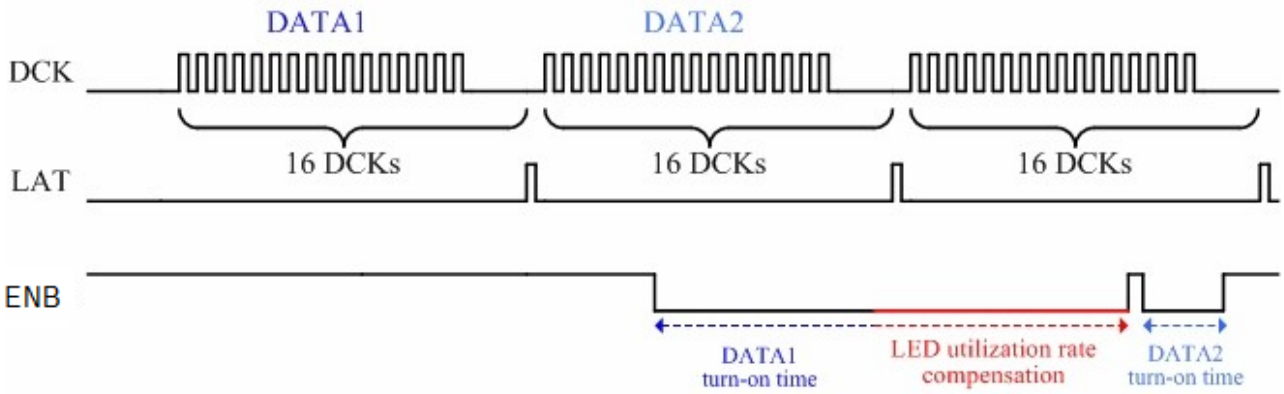
Double Latch Display Technology

CS8817 adopts the new double latch display technology to enhance display effectiveness. By saving an extra bit, CS8817 could receive a control pattern that a ENB signal extends over a LAT signal. The visual refresh rate, the LED utilization rate, the grayscale level and the low grayscale uniformity would be better than conventional pure drivers.

Convention



Double latch technology



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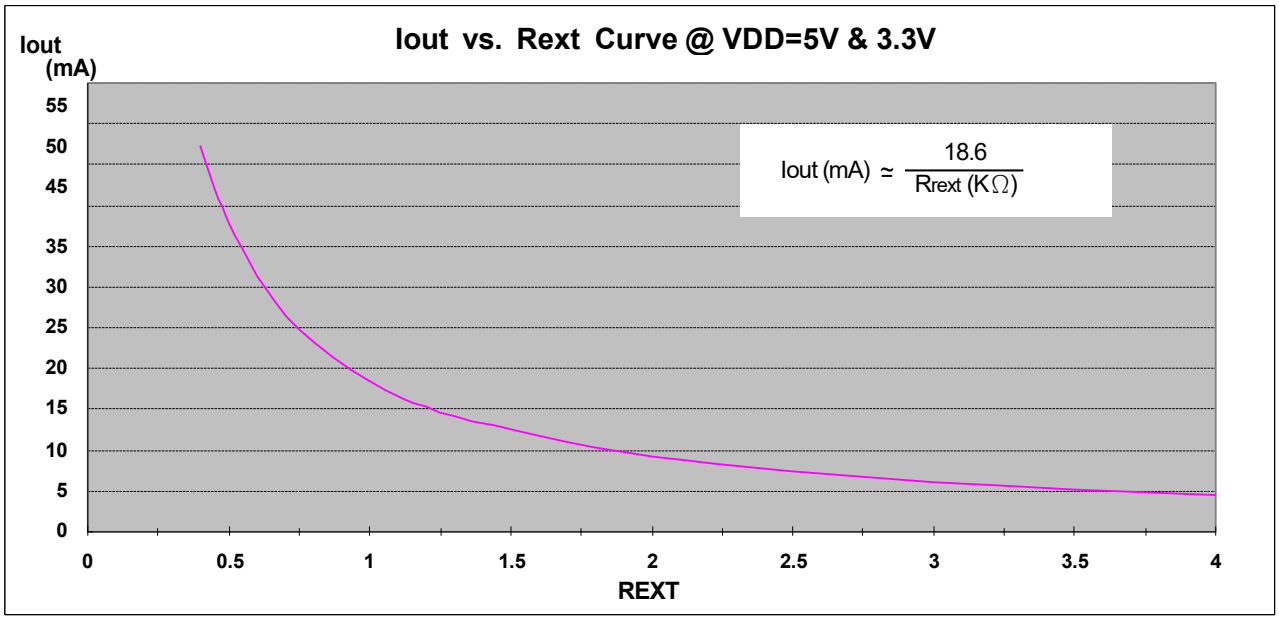
Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$Iout\ (mA) = \frac{18.6}{Rrext\ (K\Omega)}$$

Where Rrext is a resistor placed between REXT and GND
For example, Iout is 20mA when Rrext=930Ω and Iout is 5mA when Rrext=3.7KΩ



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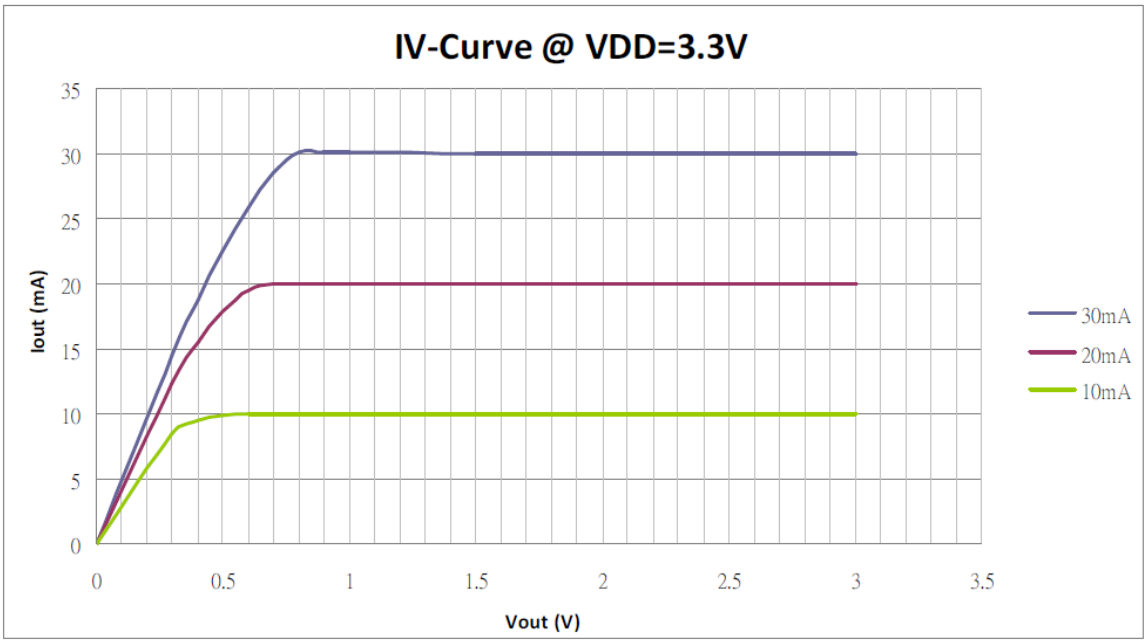
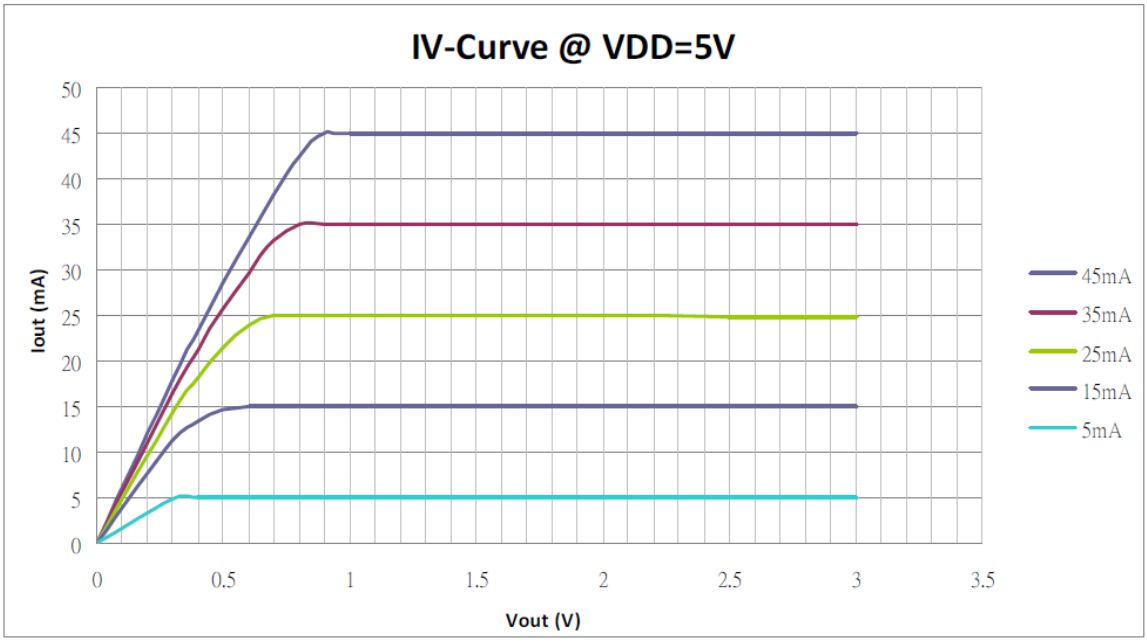
Constant-Current Output

The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the CS8817 could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.





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Power Dissipation

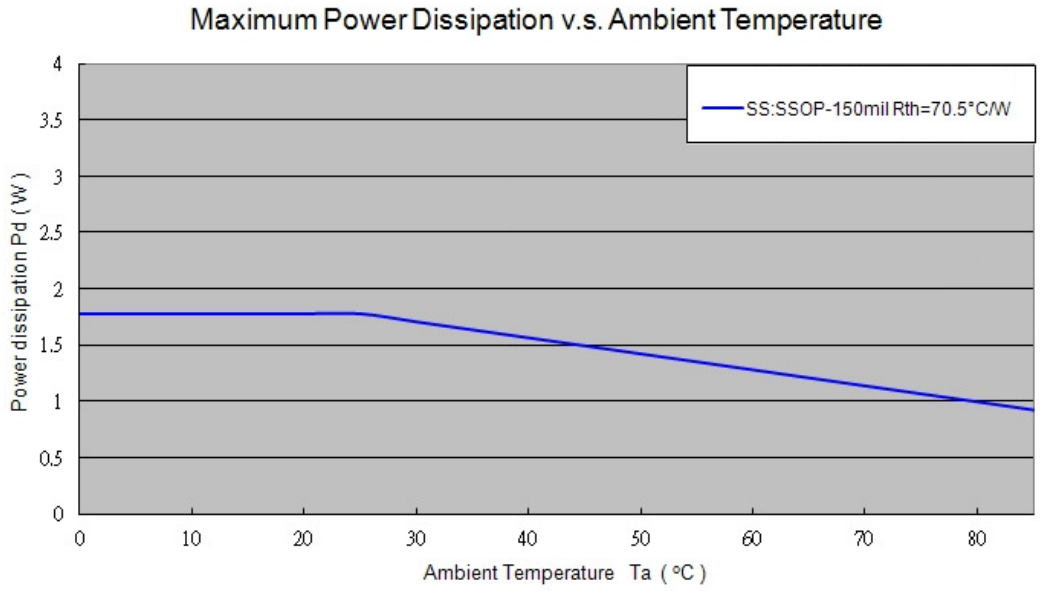
When the 16 output channels are turned on, the practical power dissipation is determined by the following equation

$$PD\ (practical) = V_{DD} \times I_{DD} + Vout_{(0,} \times Iout_{(0,} \times Duty_{(0,} + \cdots + Vout_{(N,} \times Iout_{(N,} \times Duty_{(N,}\ ,\ where\ N=1\ to\ 15$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(℃) - Ta(℃)}{Rth(j\text{-}a)(℃/Watt)}$$

The PD (max) declines as the ambient temperature rises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in these two different packages.



■ Order Information

Part No.	Package Type	Lead Pitch
CS8817AF	24SSOP(236mil)	1.0mm

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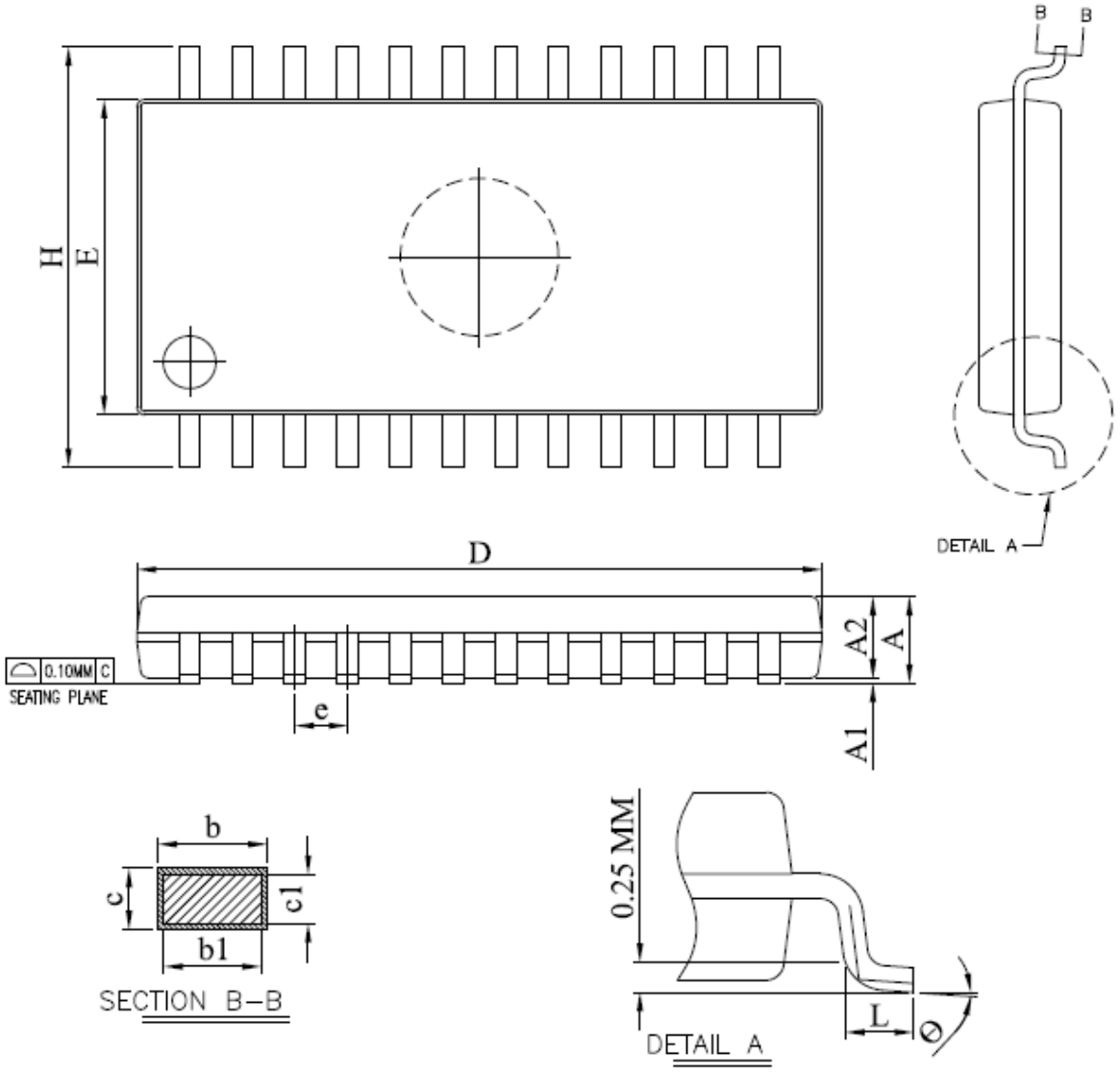
■ Package Outline

24L SSOP-236mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	e	E	H	L	θ°
mm	Min.	-	0.05	1.30	0.30	0.30	0.10	0.10	12.80	1.00 BSC	5.80	7.70	0.25	0
	Nom.	-	0.10	1.50	0.40	0.40	0.15	0.15	13.00		6.00	8.00	0.45	-
	Max.	1.90	0.15	1.70	0.52	0.50	0.27	0.25	13.20		6.20	8.30	0.65	10

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