Revision History

Rev. No.	History	Issue Date
1.0	New Issue	Nov.24, 2015

Product Description

The CS26LV64173A is a high performance, high speed, low power Pseudo SRAM organized as 4,194,304 words by 16 bits and operates from a wide range of 2.6 to 3.6V supply voltage. Advanced DRAM technology and circuit techniques provide both high speed and low power features with a maximum standby current of 150uA and maximum access time of 70ns in 2.6 to 3.6V operation. Easy memory expansion is provided by an active LOW chip enable inputs (/CE1&CE2) and active LOW output enable (/OE) and three-state output drivers. The CS26LV64173A has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS26LV64173A is available 48-pin TFBGA package.

The efficient Page Read Mode, data can be read by only changing A0-A3 when A4-A21 is fixed, while /CE1=L, CE2=H, /WE=H, /OE=L, /UB=L, /LB=L.
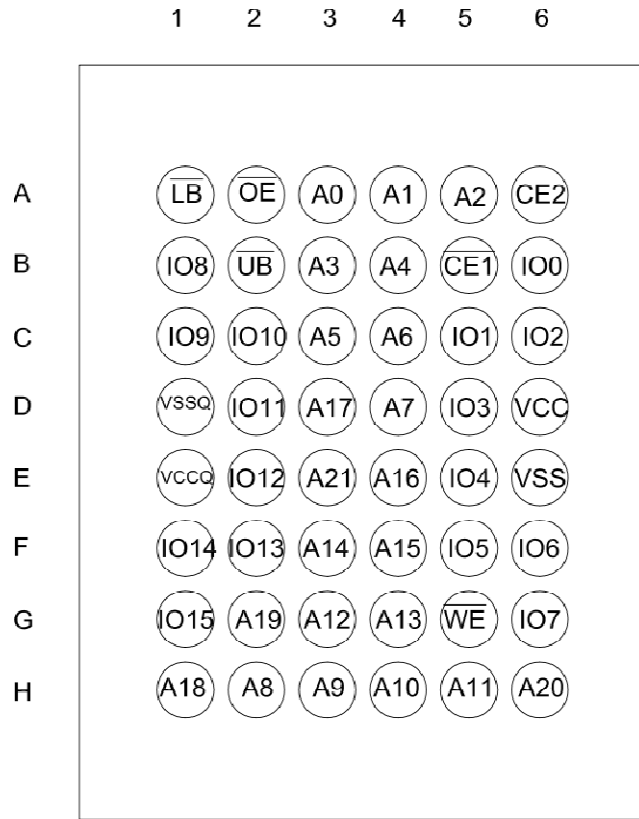
Features

- Low operation voltage: 2.6 ~ 3.6V
- Ultra low power consumption:
  - *50mA@14MHz (Max.) operating current*
  - *150uA (Max.) CMOS standby current*
- High speed access time: 70ns (Max.)
- Auto-TCSR for power saving
- Three state outputs and TTL compatible
- Deep power-down mode: Memory cell data invalid.
- Page operation mode

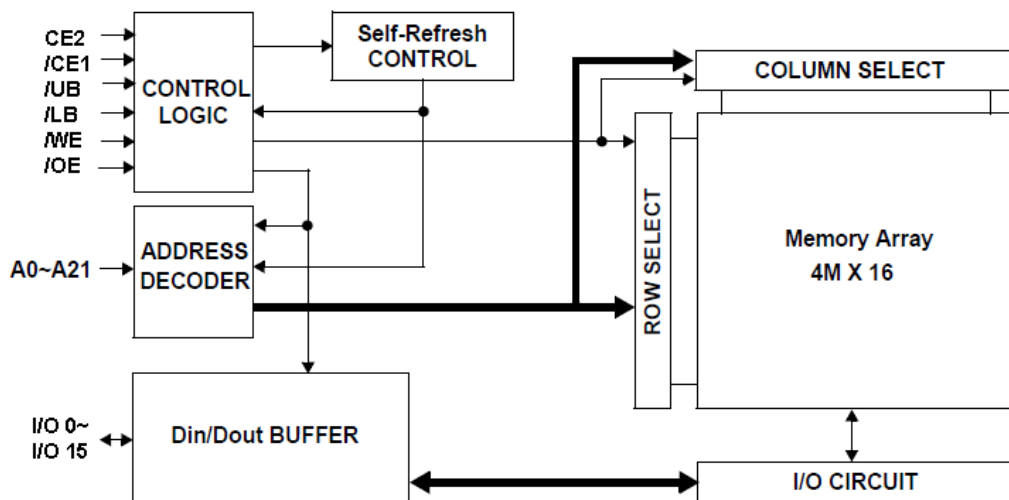## Product Family

Product Family	Operating Temp	V_{CC} Range	Speed (ns)	Standby (Max.)	Package Type
CS26LV64173A	0~70°C	2.6~3.6	70	150 uA	Dice
	-40~85°C				48 TFBGA-6x8mm

Pin Configuration

	1	2	3	4	5	6
A	LB	OE	A0	A1	A2	CE2
B	IO8	UB	A3	A4	CE1	IO0
C	IO9	IO10	A5	A6	IO1	IO2
D	VSSQ	IO11	A17	A7	IO3	VCC
E	VCCQ	IO12	A21	A16	IO4	VSS
F	IO14	IO13	A14	A15	IO5	IO6
G	IO15	A19	A12	A13	WE	IO7
H	A18	A8	A9	A10	A11	A20

Functional Block Diagram

Pin Description

Name	Type	Function
A0 ~ A21	Input	A0~A3, page address inputs, while A4~A21 address inputs
/CE1 & CE2	Input	/CE is active LOW. Chip enables must be active when data read from or write to the device. If chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
/WE	Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins; when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
/LB and /UB	Input	Lower byte and upper byte data input/output control pins.
I/O0-I/O15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
VCC	Power	Power Supply
VSS	Power	Ground

Truth Table

MODE	/CE1	CE2	/WE	/OE	/LB	/UB	IO0~7	IO8~15	VCC Current
Deep power down	X	L	X	X	X	X	High Z	High Z	I_{CCSBP}
Not Selected	H	H	X	X	X	X	High Z	High Z	I_{CCSB}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	H	L	L	L	D_{OUT}	D_{OUT}	I_{CC}
					H	L	High Z	D_{OUT}	I_{CC}
					L	H	D_{OUT}	High Z	I_{CC}
Write	L	H	L	X	L	L	D_{IN}	D_{IN}	I_{CC}
					L	H	D_{IN}	High Z	I_{CC}
					H	L	High Z	D_{IN}	I_{CC}

Absolute Maximum Ratings [(Note)]

Symbol	Parameter	Rating	Unit
V_{CC}	Power supply voltage	-0.2 to 3.6	V
V_{IN}	Input voltage	-0.2 to 3.6	V
V_{OUT}	Output voltage	-0.2 to 3.6	V
T_{BIAS}	Temperature under Bias	-40 to +85	^{O}C
T_{STG}	Storage Temperature	-65 to +150	^{O}C
P_{T}	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a

rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this

specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Ta = -40 to +85°C , V$_{CC}$ = 2.6 to 3.6V)

| Parameter Name	Parameter	Test Conduction	MIN	TYP	MAX	Unit
VIL	Input Low Voltage		-0.2		0.2*Vcc	V
VIH	Input High Voltage		0.8*Vcc		Vcc+0.2	V
IIL	Input Leakage Current	VCC=MAX, VIN=0 to VCC	-1		1	uA
IOL	Output Leakage Current	VCC=MAX, /CE=VIH, CE2=VIH, /OE=VIH or /WE=VIL, VIO=0V to VCC	-1		1	uA
VOL	Output Low Voltage	VCC=MIN, IOL = 0.5mA			0.2*Vcc	V
VOH	Output High Voltage	VCC=MIN, IOH = -0.5mA	0.8*Vcc			V
ICC1	Operating Power Supply Current	Cycle time=1us, IIO=0mA, 100% duty, /CE1≦0.2V, CE2≧VCC-0.2V, VIN≧ VCC-0.2V or VIN≦0.2V			5	mA
ICC2		Cycle time=Min, IIO=0mA, 100% duty, /CE1=VIL, CE2=VIH, VIN= VIL or VIH			50	mA
ICCP	Page Access Operating Current	/CE1≦VIL, CE2≧VIH , F=FMAX(2) IIO=0 mA, Page add. Cycling			25	mA
ICCSB	Standby Current -CMOS	/CE1 & CE2≧VCC-0.2V, Other pins=0V ~ Vcc			150	uA
ICCSBP	Deep Power-Down Standby Current	CE2≦0.2V, Other inputs=0V ~ Vcc (Max. condition: Vcc=3.6V @ 85℃)			15	uA

Capacitance (Ta = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	$V_{IN}=0V$	7	pF
C_{DQ}	Input /Output Capacitance	$V_{I/O}=0V$	7	pF

This parameter is guaranteed and not 100% tested.
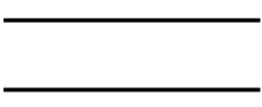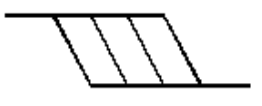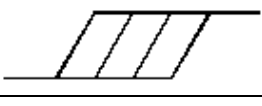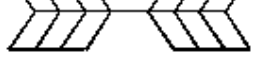
AC Test Conditions

Input Pulse Levels	V_{CC}-0.2V/0.2V
Input Rise and Fall Times	5ns
Timing Reference Level	$0.5*V_{CC}$
Output Load(See right)	$CL^{1)}$=30pF

1. Including scope and Jig capacitance.

Dout

$CL^{1)}$
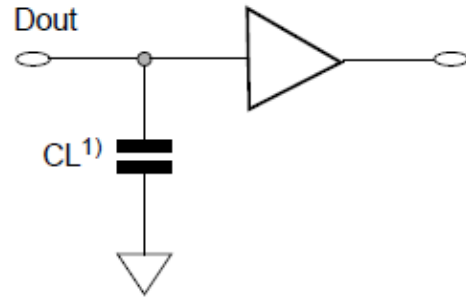
Key to Switching Waveforms

| Waveform	Inputs	Outputs
	Must be standby	Must be standby
	May change for H to L	Will be change from H to L
	May change for L to H	May change for L to H
	Don't care any change permitted	Change state unknown
	Does not apply	Center line is high impedance "OFF" state

AC Characteristics

Read cycle

Parameter Name	Name	70		Unit
		Min	Max	
Read cycle time	t_{RC}	70	10,000	ns
Address access time	t_{AA}	-	70	ns
Maximum cycle time	t_{MRC}	-	10,000	
Page read cycle time	t_{PC}	25	-	ns
Page Address Access Time	t_{PAA}	-	25	ns
Chip enable access time (/CE1)	t_{CO}	-	70	ns
Output enable to output valid (/OE)	t_{OE}	-	25	ns
Byte enable access time	t_{BA}	-	70	ns
Output hold from address change	t_{OH}	5	-	ns
Chip enable to output in low Z (/CE1)	t_{LZ}	10	-	ns
Output enable to output in low Z (/OE)	t_{OLZ}	5	-	ns
Byte enable to output in low Z	t_{BLZ}	0	-	ns
Chip disable to output in High Z (/CE1)	t_{HZ}	-	20	ns
Output disable to output in High Z (/OE)	t_{OHZ}	-	20	ns
Byte disable to output in High Z	t_{BHZ}	-	20	ns

READ CYCLE (1) (Address controlled, /CE1=/OE=VIL, CE2=/WE=VIH, /UB or/and /LB=VIL)
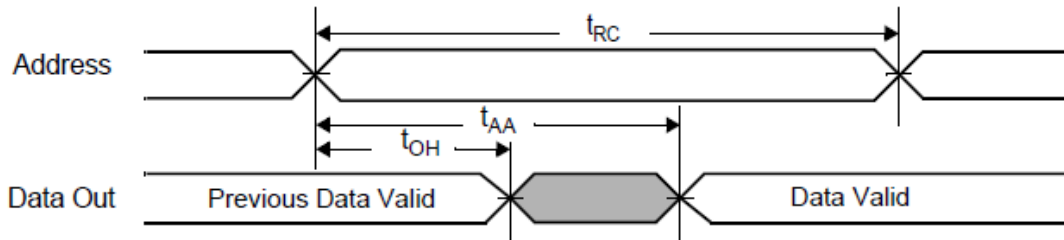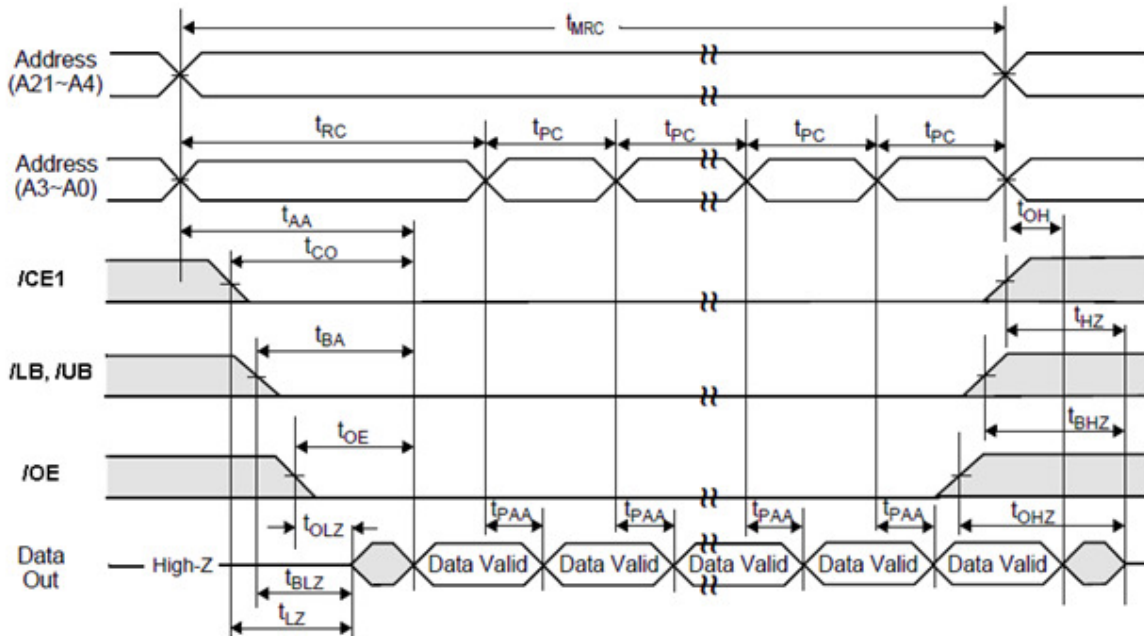
READ CYCLE (2) (CE2=/WE=VIH)
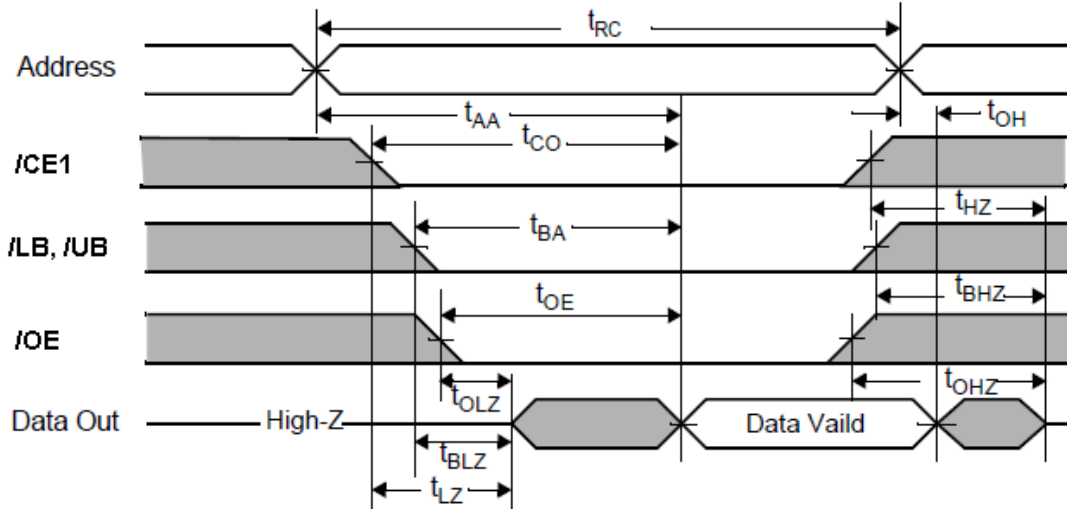
NOTE (READ CYCLE)

1. t_{HZ} , t_{BHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

2. Do not Access device with cycle timing shorter than t_{RC} for continuous periods > 10us.

PAGE READ CYCLE (3) (CE2=/WE=VIH, 16 Words access)

NOTE (READ CYCLE)

1. t_{HZ} , t_{BHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

2. Do not Access device with cycle timing shorter than t_{RC} for continuous periods > 10us.

Write Cycle

| Parameter Name	Name	70		Unit
		Min	Max	
Write cycle time	t_{WC}	70	10,000	ns
Byte enable to end of write	t_{BW}	70	-	ns
Address valid to end of write	t_{AW}	70	-	ns
Chip select to end of write	t_{CW}	70	-	ns
Data set up time	t_{DW}	25	-	ns
Data hold time	t_{DH}	0	-	ns
Write pulse width	t_{WP}	50	-	ns
Address set up time	t_{AS}	0	-	ns
Write recovery time(/WE)	t_{WR}	0	-	ns
/WE high to output low Z	t_{OW}	5	-	ns
Write to output high Z	t_{WHZ}	0	20	ns

WRITE CYCLE (1) (/WE controlled, CE2=VIH)
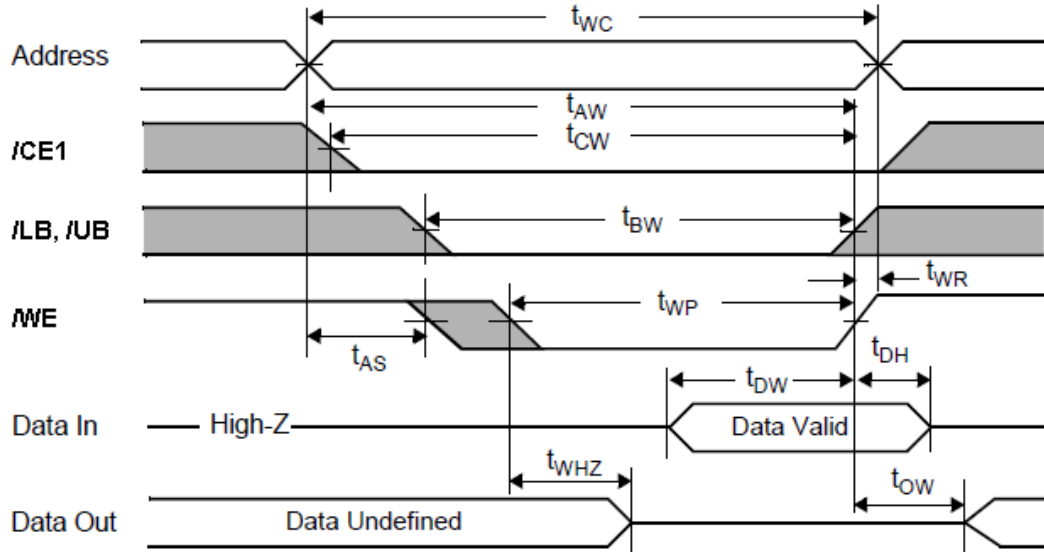
## WRITE CYCLE (2) (/CE1 controlled, CE2=VIH)
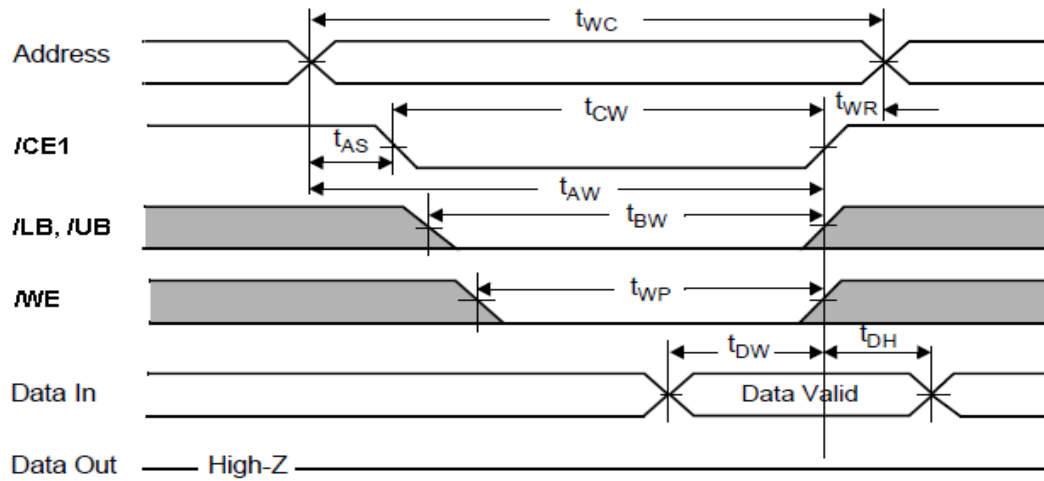
WRITE CYCLE (3) (/LB, /UB controlled, CE2=VIH)
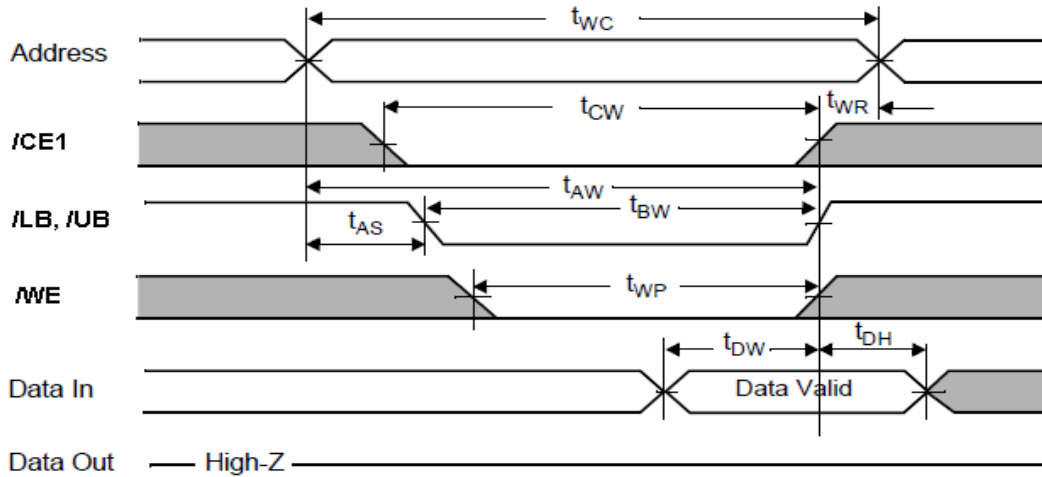
NOTE (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of low /CE1, low /WE and low /UB or /LB. A write begins at the last transition among low /CE1 and low /WE with asserting /UB or /LB low for single byte operation or simultaneously asserting /UB and /LB low for word operation. A write ends at the earliest transition among high /CE1 and high /WE. The t_{WP} is measured from the beginning of write to the end of write.

2. t_{CW} is measured from /CE1 going low to end of write.

3. t_{AS} is measured from the address valid to the beginning of write.

4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CE1 or /WE going high.

5. Do not access device with cycle timing shorter than t_{WC} for continuous periods > 10us.

Deep Power-Down Mode Entry / Exit
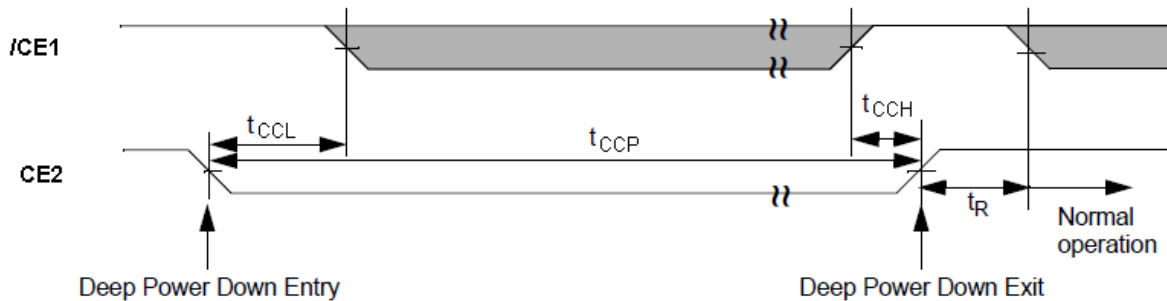
Parameter Name	Name	70		Unit
		Min	Max	
CE2 low to /CE1 low	t_{CCL}	0	-	ns
/CE1 high to CE2 high	t_{CCH}	0	-	ns
Operation Recovery Time	t_R	200	-	us
CE2 Pulse Width	t_{CCP}	20	-	ns

NOTE (DEEP POWER DOWN)

During Deep Power Down mode, all refresh related activity are disabled.

Timing Waveform of Power Up
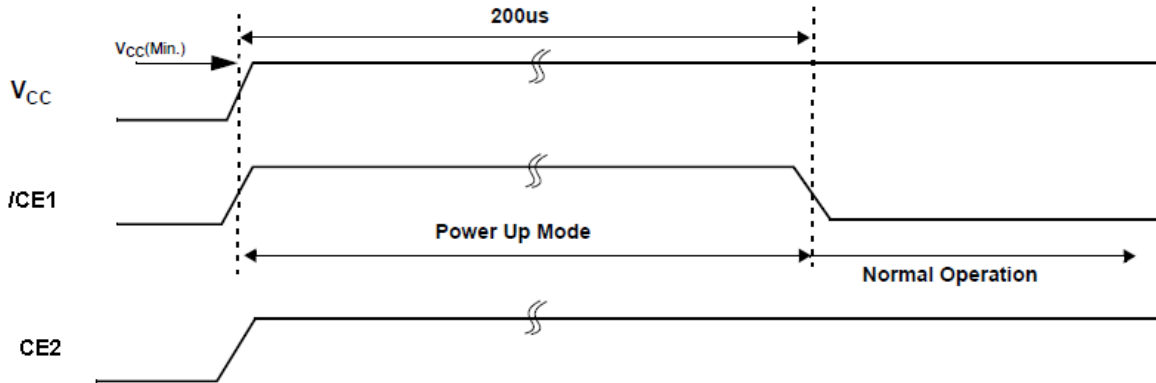
NOTE (POWER UP)

1.   *After V_{CC} reaches V_{CC} (Min.), wait 200us with /CE1 high. Then you get into the normal operation.*

Order Information

CS26LV64173A X X X X X

Package:
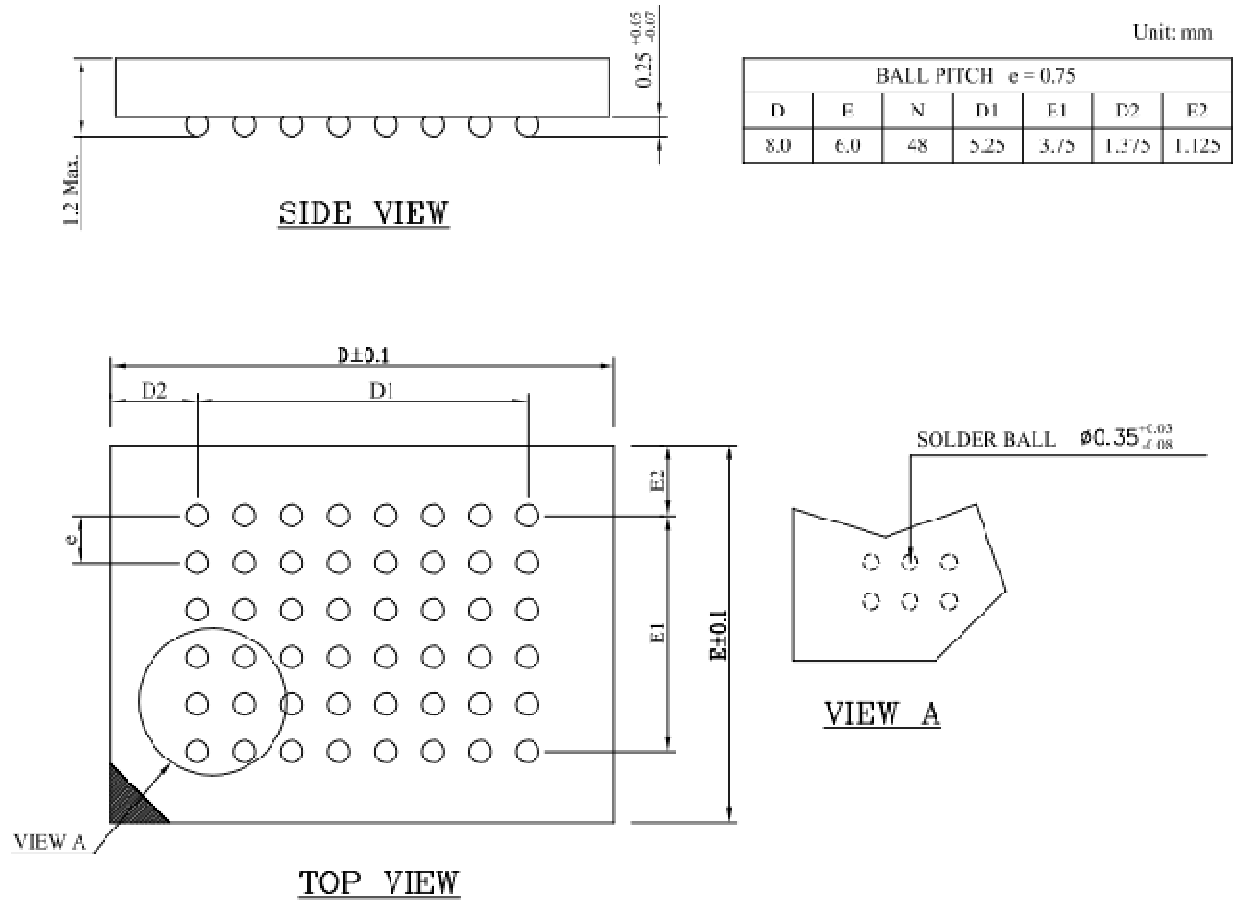H: 48 ball TFBGA-6x8mm
Z: Dice

Speed:
70: 70 ns

Temperature:
C: 0~70 °C
I: -40~85 °C

Package Material:
P: Lead Free

Note: Package material code "P" meets ROHS

Package Outline

48 ball TFBGA-6x8mm

SIDE VIEW

Unit: mm

BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125

SOLDER BALL ø0.35$^{+0.03}_{-0.08}$

VIEW A

TOP VIEW

VIEW A

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
    LINEAR : X.X = ±0.1
              X.XX = ± 0.05
              X.XXX = + 0.025