

Nano Meter Coated (NMC)SiC MOSFET

■ Features

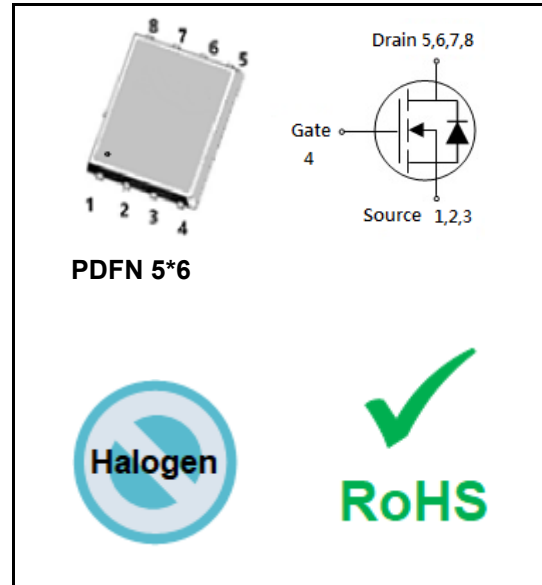
- Effectively lower down T_j and R_{th} , High anti-EMI ability
- High Speed Switching with Low Capacitances
- High Blocking Voltage with Low $R_{DS(ON)}$
- Easy to drive and parallel
- RoHS Compliant

■ Benefits

- Increased Power Density
- Higher Operating Frequency
- Reduced Heat Sink Requirements
- Higher Efficiency
- EMI Reduction

■ Applications

- Power Factor Correction Modules
- Switch Mode Power Supplies
- Power Inverters
- High Voltage Converters



Top Mark: CSiC650380T5

Ordering P/N: CSiC650380T5

Parameter	Value	Unit
V_{DS}	650	V
$I_D(T_C=25^\circ\text{C})$	12	A
$R_{DS(ON)}$	360	m Ω

■ Absolute Maximum Ratings ($T_j=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Value	Unit
V_{DS}	Drain-Source Voltage		650	V
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	12	A
		$T_C=100^\circ\text{C}$	9	A
I_{DM}	Peak Drain Current	Pulse width t_p limited by T_{jmax}	26	A
V_{GSmax}	Gate-Source Voltage		-5/26	V
V_{GSop}	Recommend Gate-Source Voltage		0/15	V
P_{tot}	Power Dissipation	$T_C=25^\circ\text{C}$	52	W
		$T_C=100^\circ\text{C}$	25	W
T_j	Operating Junction Temperature		-55~175	$^\circ\text{C}$
T_{stg}	Storage Temperature		-55~175	$^\circ\text{C}$

■ Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	$V_{GS} = 0V, I_D = 1mA$	
I_{DSS}	Zero Gate Voltage Drain Current		2	100	μA	$V_{GS} = 0V, V_{DS} = 650V$	
I_{GSS+}	Gate-Source Leakage Current			200	nA	$V_{DS} = 0V, V_{GS} = +22V$	
I_{GSS-}	Gate-Source Leakage Current			200	nA	$V_{DS} = 0V, V_{GS} = -10V$	
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.5	4.2	V	$V_{GS} = V_{DS}, I_{DS} = 1mA, T_J = 25^\circ C$	Fig. 14
			2.6			$V_{GS} = V_{DS}, I_{DS} = 1mA, T_J = 175^\circ C$	
$R_{DS(on)}$	Static Drain-Source On-Resistance		380	440	m Ω	$V_{GS} = 15V, I_D = 6A, T_J = 25^\circ C$	Fig. 15
			420			$V_{GS} = 15V, I_D = 6A, T_J = 175^\circ C$	
C_{iss}	Input Capacitance		208		pF	$V_{DS} = 400V, f = 1MHz, V_{GS} = 0V$	Fig. 8
C_{oss}	Output Capacitance		18				
C_{rss}	Reverse Transfer Capacitance		1.8				
Q_g	Total Gate Charge		10.6		nC	$V_{DD} = 400V, V_{GS} = -5/18V, I_D = 5A$	Fig. 7
Q_{gs}	Gate-Source Charge		5.1				
Q_{gd}	Gate-Drain Charge		2.2				
$R_{G(int)}$	Gate Input Resistance		1.2		Ω	$f = 1MHz, I_D = 0A$	
E_{on}	Turn-On Switching Energy		25		μJ	$V_{DD} = 400V, I_D = 5A, R_G = 10\Omega, V_{GS} = -5/18V$	Fig. 12
E_{off}	Turn-Off Switching Energy		10				
$t_{d(on)}$	Turn-On Delay Time		5		ns	$V_{DD} = 400V, I_D = 5A, R_G = 10\Omega, V_{GS} = -5/18V$	
t_r	Rise Time		17				
$t_{d(off)}$	Turn-Off Delay Time		8				
t_f	Fall Time		10				

Reverse SiC Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage		4.0		V	$V_{GS} = -4V, I_{SD} = 5A, T_J = 25^\circ C$	Fig. 16
			3.6			$V_{GS} = -4V, I_{SD} = 5A, T_J = 175^\circ C$	Fig. 17
$*I_{SD}$	Continuous Diode Forward Current			11	A	$T_C = 25^\circ C$	
				6		$T_C = 175^\circ C$	
t_{rr}	Reverse Recovery Time		50		ns	$I_{SD} = 5A,$ $di/dt = 1000A/\mu s,$ $V_{DD} = 400V, V_{GS} = -5V$	
Q_{rr}	Reverse Recovery Charge		38		nC		
I_{RRM}	Peak Reverse Recovery Current		2.4		A		

* Depends on bonding wire Φ

Thermal Data

SYMBOL	PARAMETER	Typ.	UNIT
R_{thJC}	Thermal Resistance from Junction to Case (Note Fig.2)	2.88	$^\circ C/W$
R_{thJA}	Thermal Resistance from Junction to Ambient	40	$^\circ C/W$

Typical Characteristics

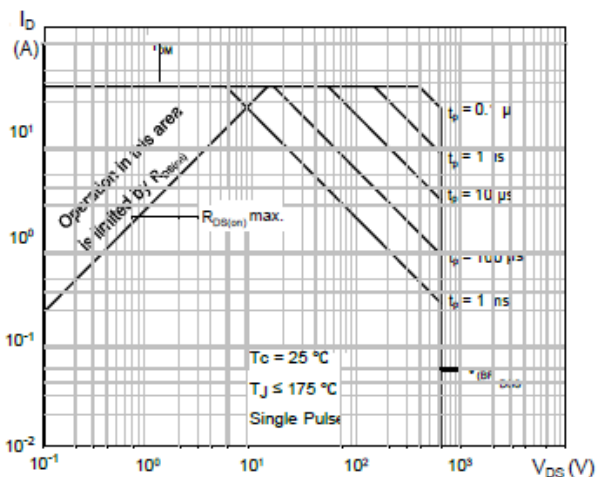


Figure 1. Safe Operating Area

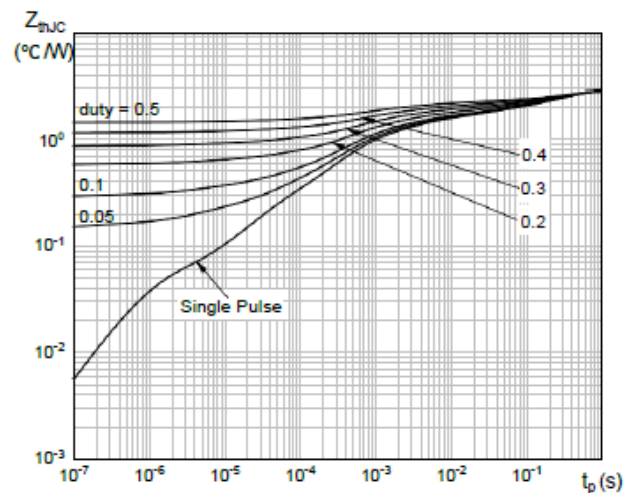


Figure 2. Maximum Transient Thermal Impedance

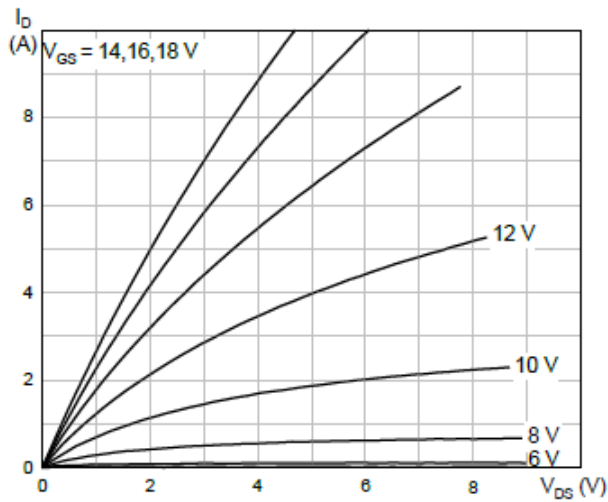


Figure 3. Typical Output Characteristics, $T_J=25^{\circ}\text{C}$

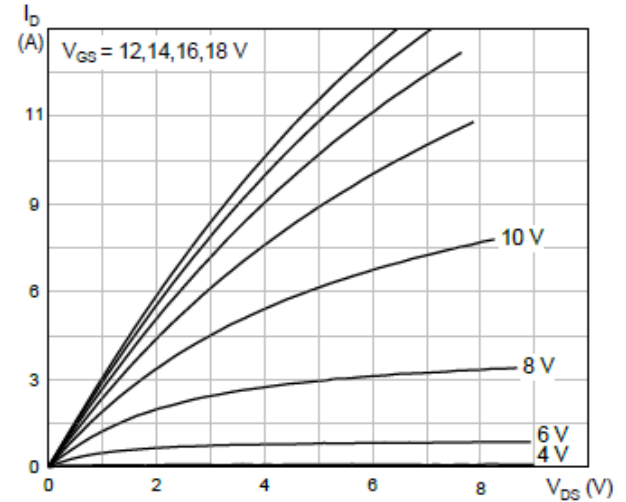


Figure 4. Typical Output Characteristics, $T_J=175^{\circ}\text{C}$

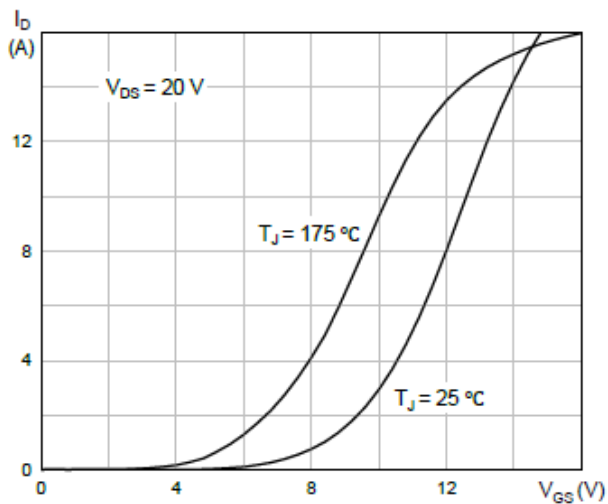


Figure 5. Typical Transfer Characteristics

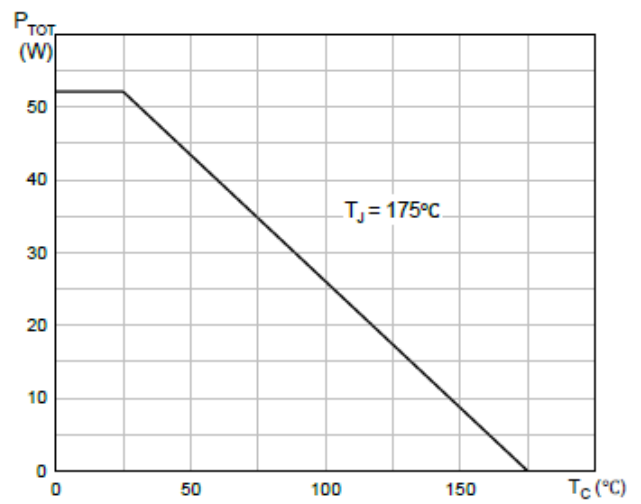


Figure 6. Total Power Dissipation

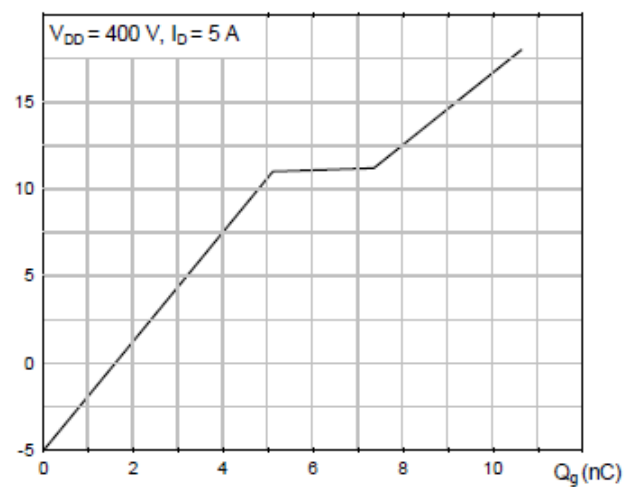


Figure 7. Typical Gate Charge Characteristics

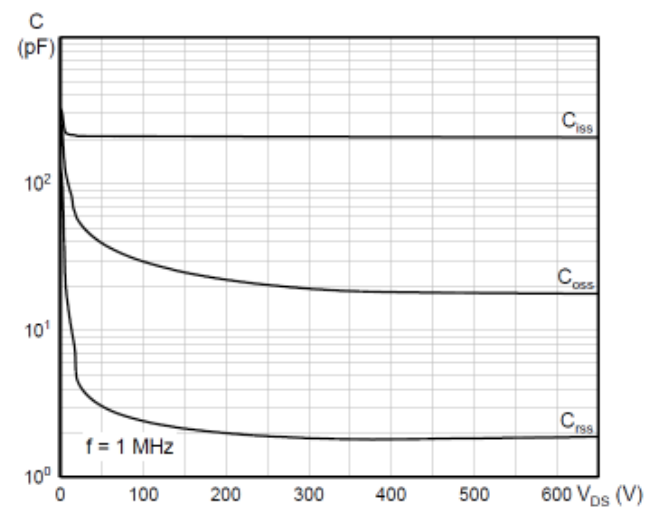


Figure 8. Typical Capacitance Characteristics

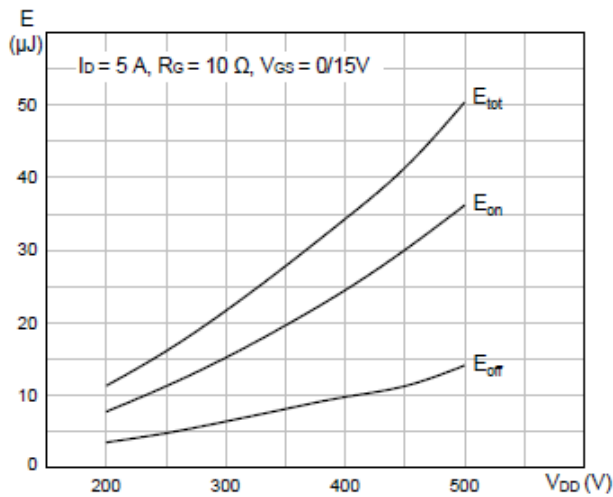


Figure 9. Typical Switching Energy vs. Supply Voltage

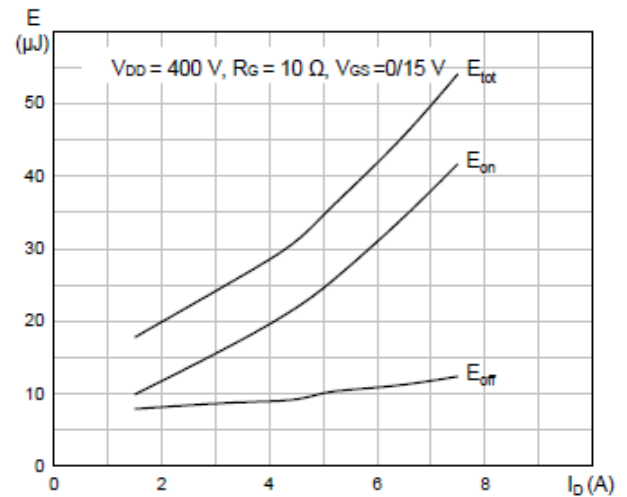


Figure 10. Typical Switching Energy vs. Drain Current

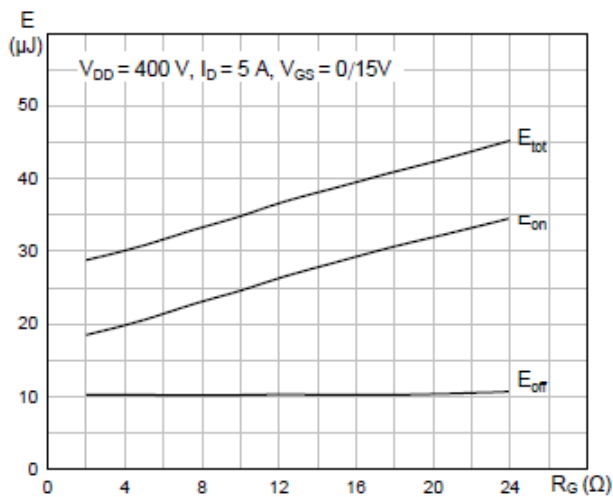


Figure 11. Switching Energy vs. Gate Resistance

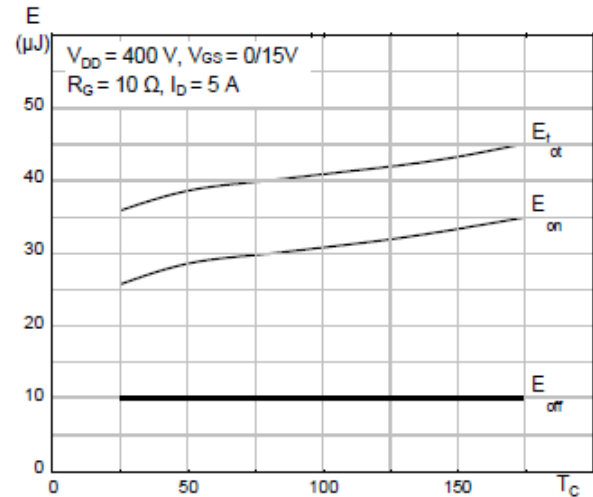


Figure 12. Typical Switching vs. Temperature

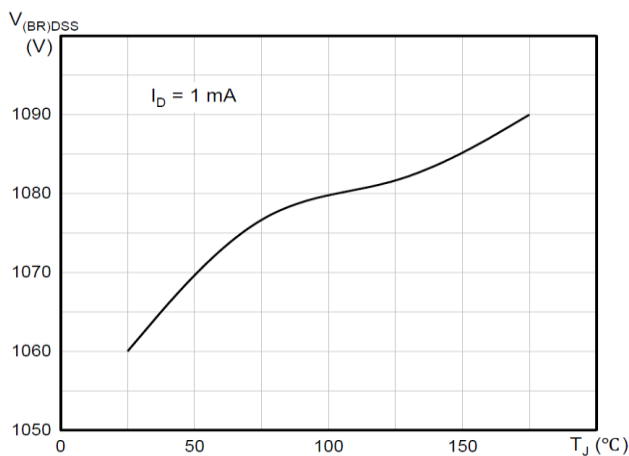


Figure 13. Breakdown Voltage vs. Temperature

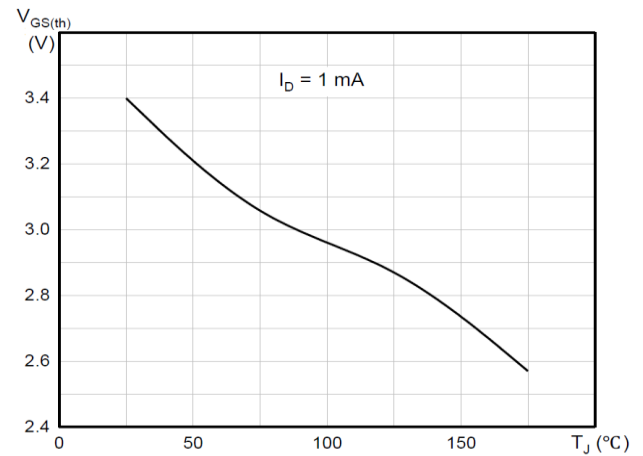


Figure 14. Gate Threshold vs. Temperature

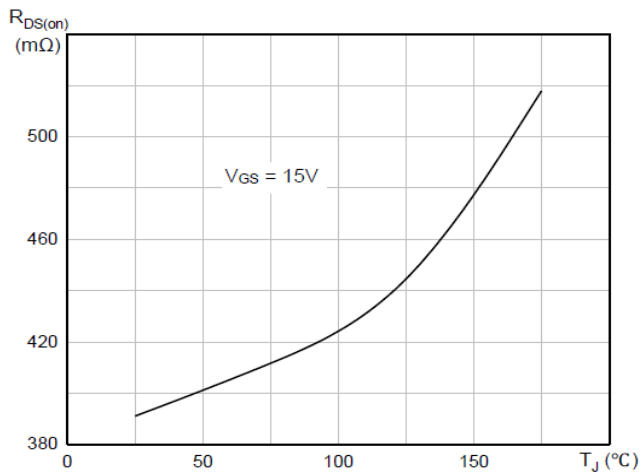


Figure 15. On-Resistance vs. Temperature

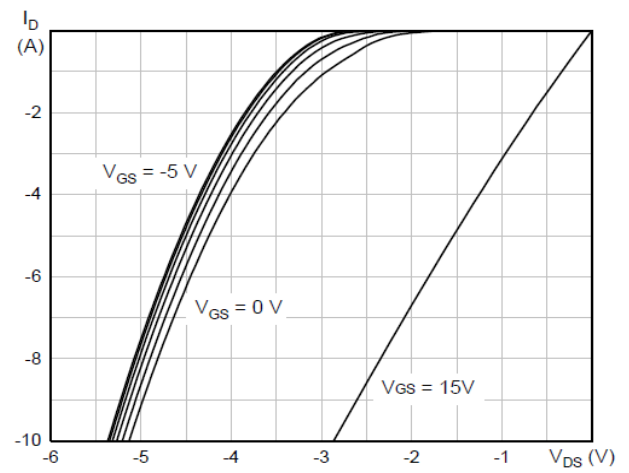


Figure 16. Body Diode Characteristics, $T_J = 25^{\circ}\text{C}$

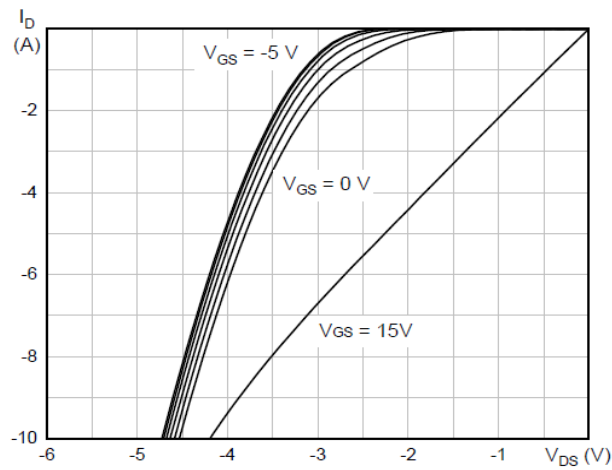


Figure 17. Body Diode Characteristics, $T_J = 175^{\circ}\text{C}$

■ Package Outline Dimension

PDFN 5*6

Technical drawing of a package showing top, side, and bottom views with dimensions L, L1, L2, A, B, C, C1, C2, E, and R.

Top View: Dimensions L (total width), L1 (inner width), and L2 (lead width) are indicated. A central circular feature is shown.

Side View: Dimensions A (height), C (lead thickness), C1 (lead width), and C2 (package thickness) are indicated. A sloped lead is shown with angle R.

Bottom View: Dimensions B (lead width), E (lead pitch), and R (lead angle) are indicated. A central circular feature is shown.

Dim.	Min.	Max.
A	4.8	5.2
B	0.25	0.35
C	1.0	1.2
C1	Typ 0.254	
C2	Typ 0.254	
E	Typ 1.27	
L	6.0	6.3
L1	5.7	6.0
L2	MAX 0.2	
R	Typ 13°	

All Dimensions in millimeter