



8M Async Fast SRAM

CS18FS8192W
CS16FS8192W

Cover Sheet and Revision Status

| 版別 (Rev.) | DCC No | 生效日 (Eff. Date) | 變更說明 (Change Description) | 發行人 (Originator) |
|--------------|-----------|--------------------|---|---------------------|
| 1.0 | | Apr.15,2014 | New issue | Hank Lin |
| 2.0 | | Nov. 8, 2021 | Revise “Chiplus reserves the right to change product or specification without notice” to “Chiplus reserves the right to change product or specification after approving by customer. ” | Hank Lin |
| 3.0 | 20240007 | May. 23, 2024 | Delete 5V products | Hank Lin |
| 4.0 | 20240018 | Oct. 22, 2024 | Corrected the minimum value of tAS and tWR from 0ns to 1.5ns | Hank Lin |



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CS16FS8192W

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CS16FS8192W

GENERAL DESCRIPTION

The CS16FS8192W and CS18FS8192W are a 8,388,608-bit high-speed Static Random Access Memory organized as 512K(1M) words by 16(8) bits. The CS16FS8192W(CS18FS8192W) uses 16(8) common input and output lines and have an output enable pin which operates faster than address access time at read cycle, And CS16FS8192W allows that lower and upper byte access by data byte control(\overline{UB} , \overline{LB}). The device is fabricated using advanced CMOS process, 6-TR based cell technology and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The CS16FS8192W and CS18FS8192W are packaged in a 400mil 44-pin TSOP2 and 48FBGA.

FEATURES

- Fast Access Time 8,10,12,15ns(Max)
- CMOS Low Power Dissipation
Standby (TTL): 25mA (Max.)
(CMOS): 15mA (Max.)
Operating: 80mA (8ns, Max..)
: 70mA(10ns ,Max.)
- Wide range (1.65V~3.6V) of Power Supply
- TTL Compatible inputs and Outputs
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control(x16 Mode)
 \overline{LB} : I/O₀~I/O₇, \overline{UB} : I/O₈~I/O₁₅
- Standard 44TSOP2 and 48FBGA Package Pin Configuration for 1Mx8
- Standard 44TSOP2 and 48FBGA Package Pin Configuration for 512Kx16
- Operating in Commercial and Industrial Temperature range.



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CS18FS8192W
CS16FS8192W

Order Information

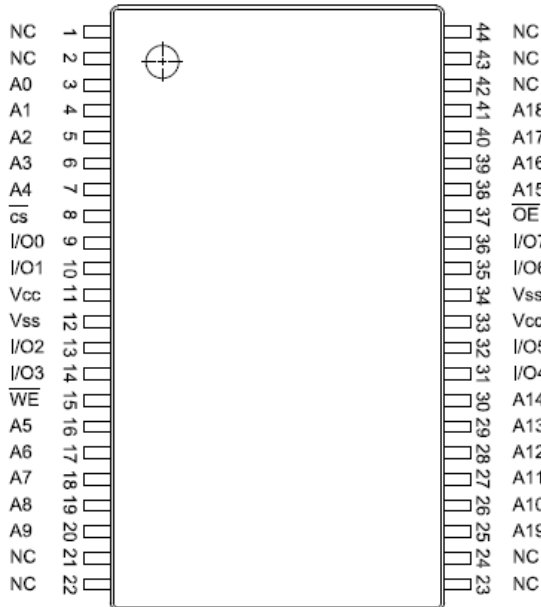
| Density | Org. | Part Number | Speed | | | Package | Temp. |
|---------|---------|----------------------|---------------------|----------------------|----------------------|----------|----------------------------------|
| | | | V _{CC} (V) | t _{AA} (ns) | t _{OE} (ns) | | |
| 8Mb | 512Kx16 | CS16FS8192WGC(I)-08* | 3.3 | 8 | 4 | 44 TSOP2 | C : Commercial I : Industrial |
| | | | 2.5 | 10 | 5 | 44 TSOP2 | |
| | | | 1.8 | 12 | 6 | 44 TSOP2 | |
| | | CS16FS8192WHC(I)-08* | 3.3 | 8 | 4 | 48 FBGA | |
| | | | 2.5 | 10 | 5 | 48 FBGA | |
| | | | 1.8 | 12 | 6 | 48 FBGA | |
| | | CS16FS8192WGC(I)-10* | 3.3 | 10 | 5 | 44 TSOP2 | |
| | | | 2.5 | 10 | 5 | 44 TSOP2 | |
| | | | 1.8 | 12 | 6 | 44 TSOP2 | |
| | | CS16FS8192WHC(I)-10* | 3.3 | 10 | 5 | 48 FBGA | |
| | | | 2.5 | 10 | 5 | 48 FBGA | |
| | | | 1.8 | 12 | 6 | 48 FBGA | |

| Density | Org. | Part Number | Speed | | | Package | Temp. |
|---------|------|----------------------|---------------------|----------------------|----------------------|----------|----------------------------------|
| | | | V _{CC} (V) | t _{AA} (ns) | t _{OE} (ns) | | |
| 8Mb | 1Mx8 | CS18FS8192WGC(I)-08* | 3.3 | 8 | 4 | 44 TSOP2 | C : Commercial I : Industrial |
| | | | 2.5 | 10 | 5 | 44 TSOP2 | |
| | | | 1.8 | 12 | 6 | 44 TSOP2 | |
| | | CS18FS8192WHC(I)-08* | 3.3 | 8 | 4 | 48 FBGA | |
| | | | 2.5 | 10 | 5 | 48 FBGA | |
| | | | 1.8 | 12 | 6 | 48 FBGA | |
| | | CS18FS8192WGC(I)-10* | 3.3 | 10 | 5 | 44 TSOP2 | |
| | | | 2.5 | 10 | 5 | 44 TSOP2 | |
| | | | 1.8 | 12 | 6 | 44 TSOP2 | |
| | | CS18FS8192WHC(I)-10* | 3.3 | 10 | 5 | 48 FBGA | |
| | | | 2.5 | 10 | 5 | 48 FBGA | |
| | | | 1.8 | 12 | 6 | 48 FBGA | |

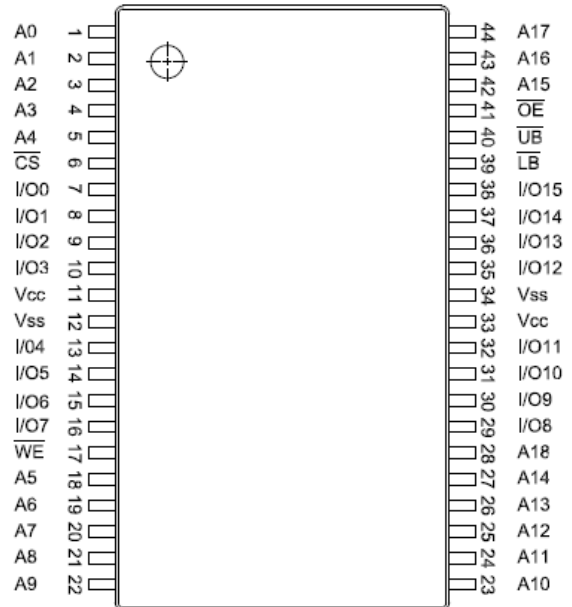
*means max. speed

PIN CONFIGURATIONS

44TSOP2-400mil



CS18FS8192(3/5/W)- (1M x 8)



CS16FS8192(3/5/W)- (512k x 16)

6x8mm mini-BGA with ball pitch 0.75mm

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----|----|-----|-----|-----|-----|
| A | NC | OE | A0 | A1 | A2 | NC |
| B | NC | NC | A3 | A4 | CS | IO0 |
| C | NC | NC | A5 | A6 | IO1 | IO2 |
| D | Vss | NC | A17 | A7 | IO3 | Vcc |
| E | Vcc | NC | NC | A16 | IO4 | Vss |
| F | NC | NC | A14 | A15 | IO5 | IO6 |
| G | NC | NC | A12 | A13 | WE | IO7 |
| H | A18 | A8 | A9 | A10 | A11 | A19 |

CS18FS8192W – (1M x 8)
48ball mini-BGA

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------|------|-----|-----|-----|-----|
| A | LB | OE | A0 | A1 | A2 | NC |
| B | IO8 | UB | A3 | A4 | CS | IO0 |
| C | IO9 | IO10 | A5 | A6 | IO1 | IO2 |
| D | Vss | IO11 | A17 | A7 | IO3 | Vcc |
| E | Vcc | IO12 | NC | A16 | IO4 | Vss |
| F | IO14 | IO13 | A14 | A15 | IO5 | IO6 |
| G | IO15 | NC | A12 | A13 | WE | IO7 |
| H | A18 | A8 | A9 | A10 | A11 | NC |

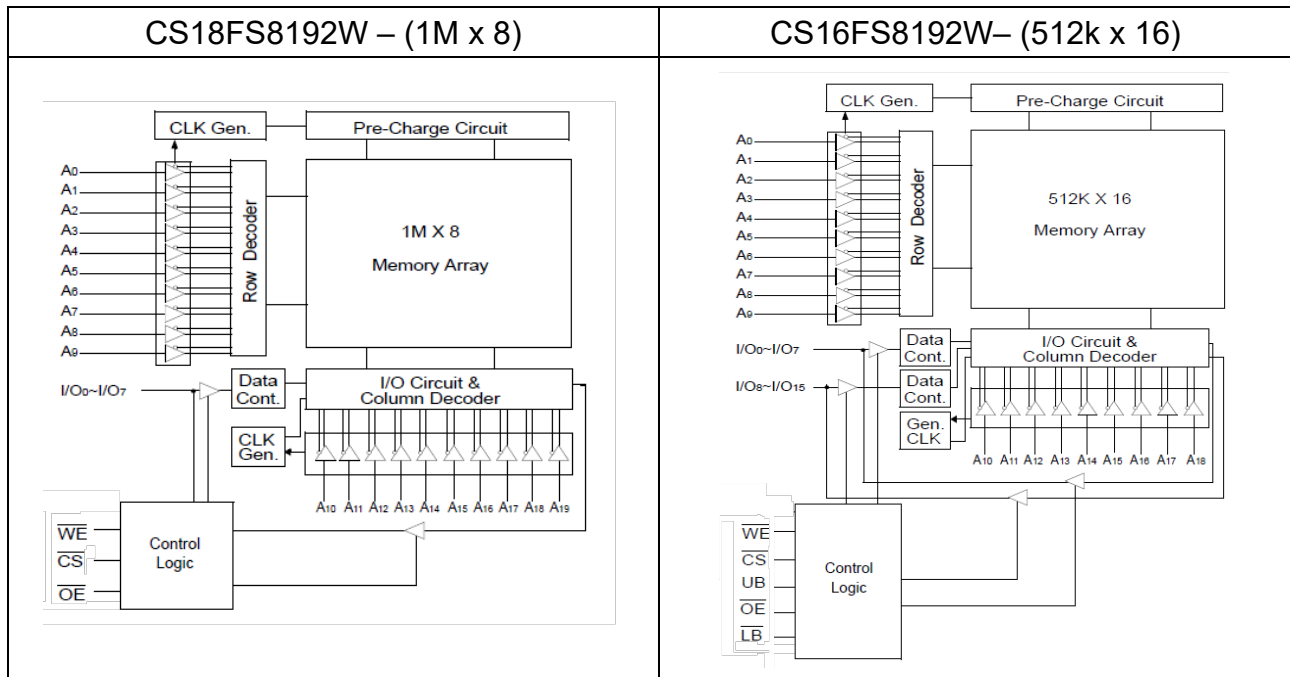
CS16FS8192W – (512k x 16)
48ball mini-BGA



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CS16FS8192W

FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings*

| Parameter | | Symbol | Rating | Unit |
|---|---------------------------------|------------------------------------|-------------------------------|------|
| Voltage on Any Pin Relative to V _{SS} | 3.3V Product | V _{in} , V _{OUT} | -0.5 to V _{CC} +0.5V | V |
| | Wide V _{CC} ** Product | | | |
| Voltage on V _{CC} Supply Relative to V _{SS} | 3.3V Product | V _{in} , V _{OUT} | -0.5 to 4.0 | V |
| | Wide V _{CC} ** Product | | -0.5 to 4.0 | |
| Power Dissipation | | P _D | 1.0 | W |
| Storage Temperature | | T _{STG} | -65 to 150 | °C |
| Operating Temperature Commercial | | T _A | 0 to 70 | °C |
| Industrial | | T _A | -40 to 85 | °C |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Wide VCC Range is 1.65V~3.6V



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Recommended DC Operating Conditions*(T_A=0 to 70°C)

| Parameter | Operating V _{CC} (V) | Symbol | Min. | Typ. | Max. | Unit |
|--------------------|-------------------------------|-----------------|------|---------|----------------------|------|
| Supply Voltage | 3.3 | V _{CC} | 3.0 | 3.3 | 3.6 | |
| | Wide 2.4~3.6 | V _{CC} | 2.4 | 2.5/3.3 | 3.6 | |
| | Wide 1.65~2.2 | V _{CC} | 1.65 | 1.8 | 2.2 | |
| Ground | | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | 3.3 | V _{IH} | 2.0 | - | V _{CC} +0.5 | |
| | Wide 2.4~3.6 | V _{IH} | 2.0 | - | V _{CC} +0.3 | |
| | Wide 1.65~2.2 | V _{IH} | 1.4 | - | V _{CC} +0.2 | |
| Input Low Voltage | 3.3 | V _{IL} | -0.3 | - | 0.8 | |
| | Wide 2.4~3.6 | V _{IL} | -0.3 | - | 0.7 | |
| | Wide 1.65~2.2 | V _{IL} | -0.2 | - | 0.4 | |

*The above parameters are also guaranteed for industrial temperature range.

DC and Operating Characteristics*(T_A=0 to 70°C)

| Parameter | Symbol | Test Conditions | Min | Max | Unit | |
|--------------------------|------------------|--|------|-----|------|----|
| Input Leakage Current | I _{LI} | V _{IN} =V _{SS} to V _{CC} | -2 | 2 | uA | |
| Output Leakage Current** | I _{LO} | $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{OUT} =V _{SS} to V _{CC} | -2 | 2 | uA | |
| Operating Current** | I _{CC} | Min.Cycle, 100% Duty $\overline{CS} = V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} = 0mA | 8ns | - | 80 | mA |
| | | | 10ns | | 70 | |
| | | | 12ns | | 65 | |
| | | | 15ns | | 60 | |
| Standby Current | I _{SB} | Min. Cycle, $\overline{CS} = V_{IH}$ | - | 25 | mA | |
| | I _{SB1} | f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$ V _{IN} ≥V _{CC} -0.2V or V _{in} ≤0.2V | - | 15 | | |
| Output Low Voltage | V _{OL} | V _{CC} =3.0V, I _{OL} =8mA, 3.3V Product & Wide V _{CC} ** Product | - | 0.4 | V | |



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CS16FS8192W

| | | | | | |
|---------------------------|-----------------|---|-----|-----|---|
| Level | | V _{CC} =2.4V, I _{OL} =1mA, Wide V _{CC} ** Product | - | 0.4 | |
| | | V _{CC} =1.65V, I _{OL} =0.1mA, Wide V _{CC} ** Product | - | 0.2 | |
| Output High Voltage Level | V _{OH} | V _{CC} =3.0V, I _{OH} = -4mA, 3.3V Product & Wide V _{CC} ** Product | 2.4 | - | V |
| | | V _{CC} =2.4V, I _{OH} = -1mA, Wide V _{CC} ** Product | 1.8 | - | |
| | | V _{CC} =1.65V, I _{OH} = -0.1mA, Wide V _{CC} ** Product | 1.4 | - | |

*The above parameters are also guarantee for industrial temperature range.

**Wide V_{CC} Range is 1.65V ~ 3.6V

Capacitance*(T_A= 25°C, f= 1.0MHz)

| Item | Symbol | Test Conditions | TYP | Max | Unit |
|---------------------------|------------------|----------------------|-----|-----|------|
| Input/ Output Capacitance | C _{I/O} | V _{I/O} =0V | - | 8 | pF |
| Input Capacitance | C _{IN} | V _{IN} =0V | - | 6 | pF |

*Capacitance is sampled and not 100% tested.

Test Conditions*

| Parameter | Value |
|--|---|
| Input/ Output Capacitance | 0 to 3.0V (V _{CC} =3.3V) |
| | 0 to 2.5V (V _{CC} =2.5V) |
| | 0 to 1.8V (V _{CC} =1.8V) |
| Input Rise and Fall Time | 1V/1ns |
| Input and Output Timing Reference Levels | 1.5V (V _{CC} =3.3V) |
| | 1/2V _{CC} (V _{CC} = 1.8V or 2.5V) |
| Output Load | See Fig. 1 |

*The above parameters are also guaranteed for industrial temperature range.

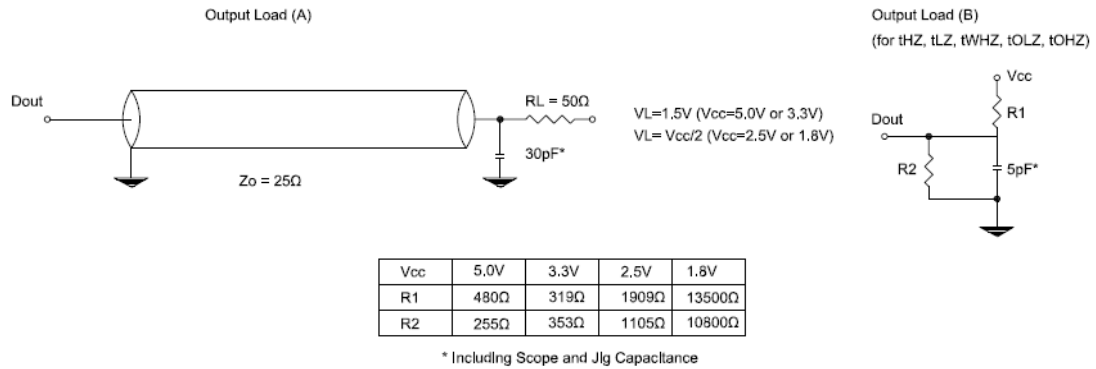
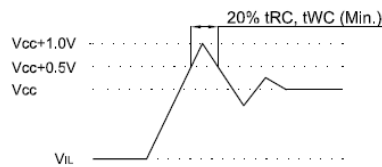


Fig 1

Overshoot Timing



Undershoot Timing

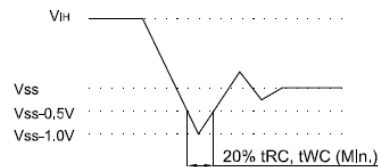


Fig 2

Functional Description (x8 Mode)

| \overline{CS} | \overline{WE} | \overline{OE} | Mode | I/O Pin | Supply Current |
|-----------------|-----------------|-----------------|----------------|-----------|-------------------|
| H | X | X* | Not Select | High-Z | I_{SB}, I_{SB1} |
| L | H | H | Output Disable | High-Z | I_{CC} |
| L | H | L | Read | D_{OUT} | I_{CC} |
| L | L | X | Write | D_{IN} | I_{CC} |

*X means don't care



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Functional Description (x16 Mode)

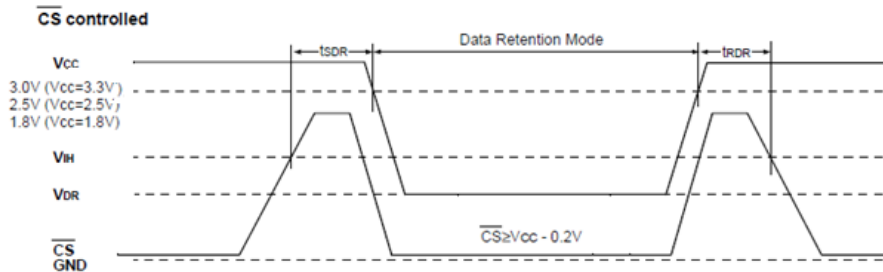
| \overline{CS} | \overline{WE} | \overline{OE} | \overline{LB}^{**} | \overline{UB}^{**} | Mode | I/O Pin | | Supply Current |
|-----------------|-----------------|-----------------|----------------------|----------------------|----------------|------------------------------------|-------------------------------------|------------------------------------|
| | | | | | | I/O ₀ ~I/O ₇ | I/O ₈ ~I/O ₁₅ | |
| H | X | X* | X | X | Not Select | High-Z | High-Z | I _{SB} , I _{SB1} |
| L | H | H | X | X | Output Disable | High-Z | High-Z | I _{CC} |
| L | X | X | H | H | | | | |
| L | H | L | L | H | Read | D _{OUT} | High-Z | I _{CC} |
| | | | H | L | | High-Z | D _{OUT} | |
| | | | L | L | | D _{OUT} | D _{OUT} | |
| L | L | X | L | H | Write | D _{IN} | High-Z | I _{CC} |
| | | | H | L | | High-Z | D _{IN} | |
| | | | L | L | | D _{IN} | D _{IN} | |

*X means don't care

Data Retention Characteristics*(T_A=0 to 70°C)

| Parameter | Product | Operating V _{CC} (V) | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|------------------------------------|--------------------|-------------------------------|------------------|--|--|------|------|------|
| V _{CC} for Data Retention | Wide 2.4V~3.6V | 2.5/3.3 | V _{DR} | $\overline{CS} \geq V_{CC} - 0.2V$ | 2.0 | - | 3.6 | V |
| | Wide 1.65V~2.2V | 1.8 | | | 1.5 | - | 3.6 | |
| Data Retention Current | Wide 2.4V~3.6V | 2.5/3.3 | I _{DR} | V _{CC} =2.0V $\overline{CS} \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V | | | 15 | mA |
| | Wide 1.65V~2.2V | 1.8 | | | V _{CC} =1.5V, $\overline{CS} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V | | | |
| Data Retention Set-Up Time | | | t _{SDR} | See Data | 0 | - | - | nS |
| Recovery Time | | | t _{RDR} | Retention Wave form (below) | 5 | - | - | mS |

Data Retention Wave form



Read Cycle*

| Parameter | Symbol | 8ns | | 10ns | | 12ns | | 15ns | | Unit |
|---|------------------|-----|-----|------|-----|------|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | t _{RC} | 8 | - | 10 | - | 12 | - | 15 | - | ns |
| Address Access Time | t _{AA} | - | 8 | - | 10 | - | 12 | - | 15 | ns |
| Chip Select to Output | t _{CO} | - | 8 | - | 10 | - | 12 | - | 15 | ns |
| Output Enable to Valid Output | t _{OE} | - | 4 | - | 5 | - | 6 | - | 7 | ns |
| $\overline{UB}, \overline{LB}$ Access Time** | t _{BA} | - | 4 | - | 5 | - | 6 | - | 7 | ns |
| Chip Enable to Low-Z Output | t _{LZ} | 3 | - | 3 | - | 3 | - | 3 | - | ns |
| Output Enable to Low-Z Output | t _{OLZ} | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| $\overline{UB}, \overline{LB}$ Enable to Low-Z Output** | t _{BLZ} | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Chip Disable to High-Z Output | t _{HZ} | 0 | 4 | 0 | 5 | 0 | 6 | 0 | 7 | ns |
| Output Disable to High-Z Output | t _{OHZ} | 0 | 4 | 0 | 5 | 0 | 6 | 0 | 7 | ns |
| $\overline{UB}, \overline{LB}$ Disable to High-Z Output** | t _{BHZ} | 0 | 4 | 0 | 5 | 0 | 6 | 0 | 7 | ns |
| Output Hold from Address Change | t _{OH} | 3 | - | 3 | - | 3 | - | 3 | - | ns |



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| | | | | | | | | | | |
|--------------------------------|-----------------|---|---|---|----|---|----|---|----|----|
| Chip Selection Power Up Time | t _{PU} | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Chip Selection Power Down Time | t _{PD} | - | 8 | - | 10 | - | 12 | - | 15 | ns |

*The above parameters are also guaranteed for industrial temperature range.

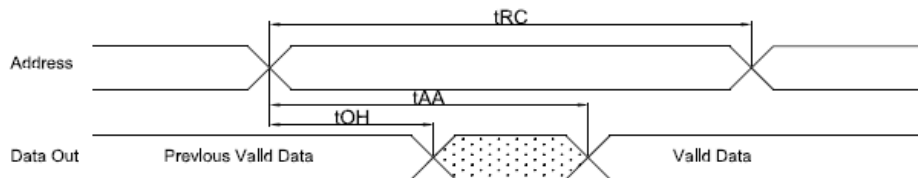
Write Cycle*

| Parameter | Symbol | 8ns | | 10ns | | 12ns | | 15ns | | Unit |
|---|------------------|-----|-----|------|-----|------|-----|------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | t _{wc} | 8 | - | 10 | - | 12 | - | 15 | - | ns |
| Chip Select to End of Write | t _{cw} | 6 | - | 7 | - | 9 | - | 12 | - | ns |
| Address Set-up Time | t _{AS} | 1.5 | - | 1.5 | - | 1.5 | - | 1.5 | - | ns |
| Address Valid to End of Write | t _{AW} | 6 | - | 7 | - | 9 | - | 12 | - | ns |
| Write Pulse Width(\overline{OE} High) | t _{WP} | 6 | - | 7 | - | 9 | - | 12 | - | ns |
| Write Pulse Width(\overline{OE} Low) | t _{WP1} | 8 | - | 10 | - | 12 | - | 15 | - | ns |
| \overline{UB} , \overline{LB} Valid to End of Write** | t _{BW} | 6 | - | 7 | - | 9 | - | 12 | - | ns |
| Write Recovery Time | t _{WR} | 1.5 | - | 1.5 | - | 1.5 | - | 1.5 | - | ns |
| Write to Output High-Z | t _{WHZ} | 0 | 4 | 0 | 5 | 0 | 6 | 0 | 7 | ns |
| Data to Write Time Overlap | t _{DW} | 4 | - | 5 | - | 7 | - | 8 | - | ns |
| Data Hold from Write Time | t _{DH} | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| End of Write to Output Low-Z | t _{OW} | 3 | - | 3 | - | 3 | - | 3 | - | ns |

*The above parameters are also guaranteed for industrial temperature range.

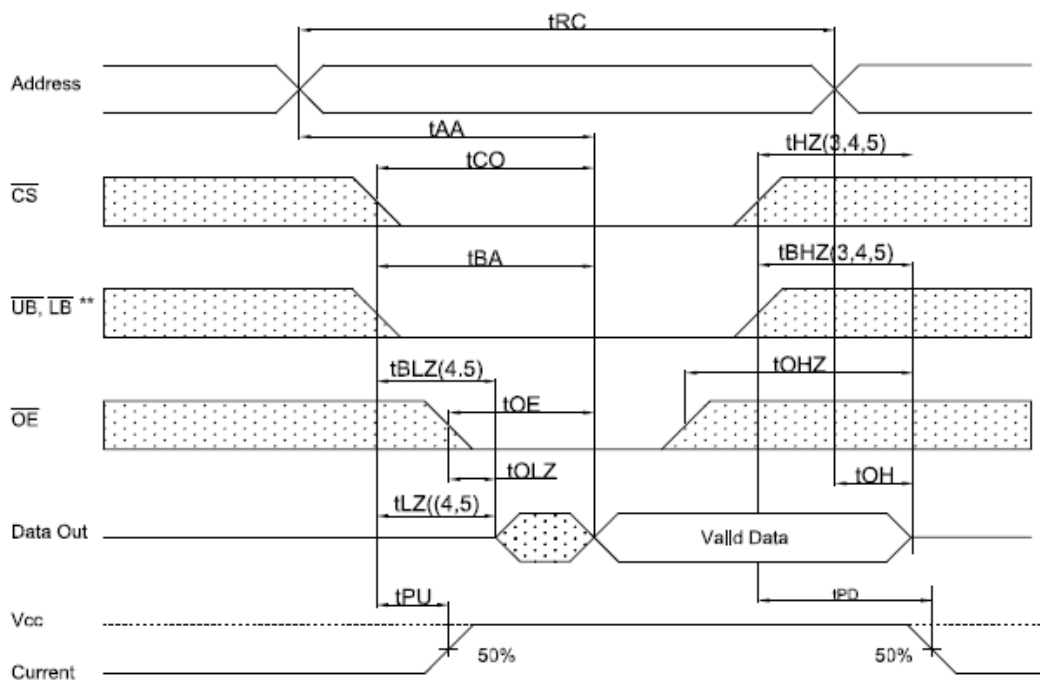
Timing Diagram

Timing Waveform of Read Cycle (1) (Address Controlled, $\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, \overline{UB} , $\overline{LB} = V_{IL}$ **)



** Those parameters are applied for x16 mode only.

Timing Waveform of Read Cycle (2) ($\overline{WE} = V_{IH}$)



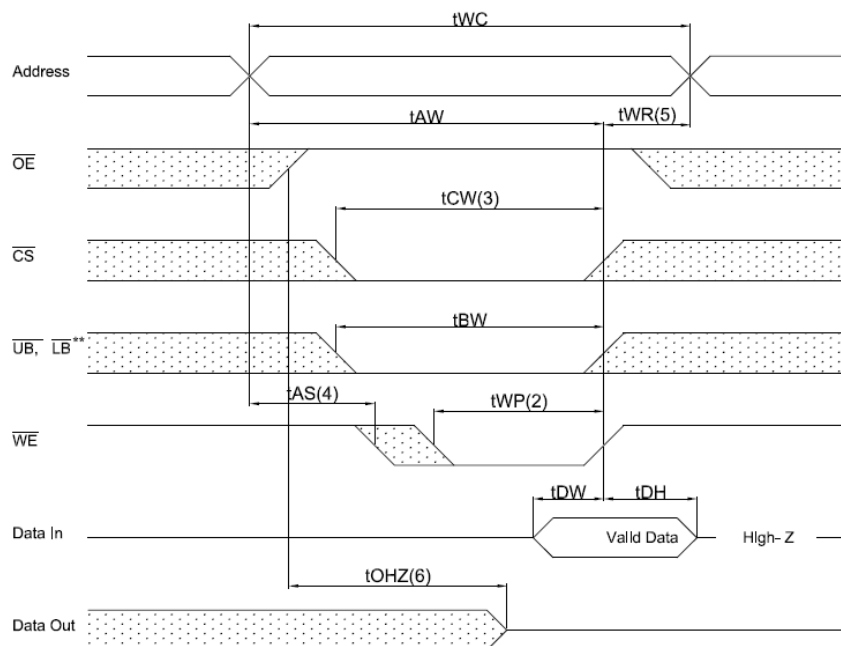
NOTES (Read Cycle)

1. \overline{WE} is high for read cycle
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

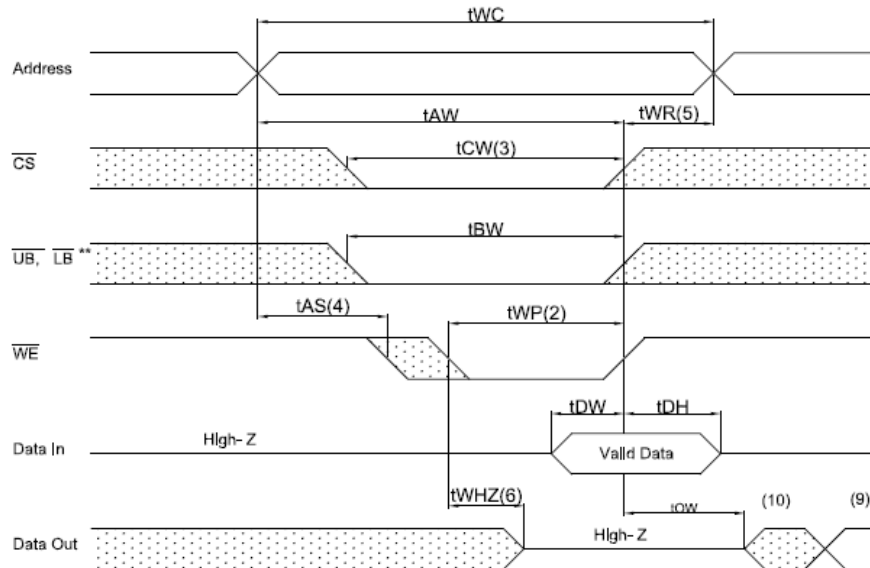
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (1) (\overline{OE} Clock)



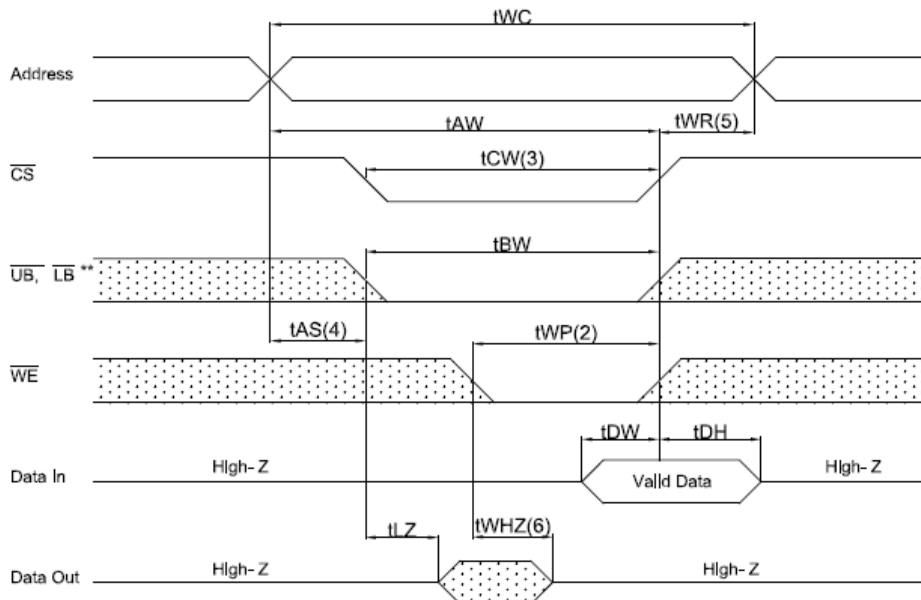
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (2) (\overline{OE} = Low fixed)



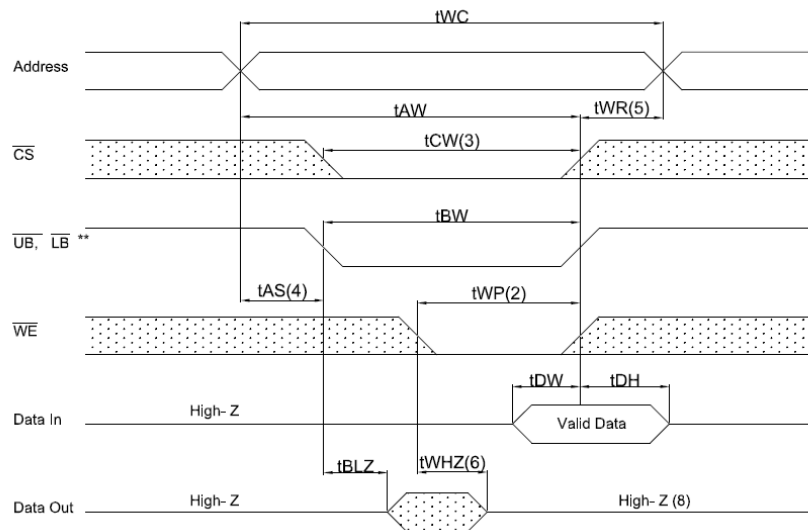
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (3) (\overline{CS} = Controlled)



** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (4) (\overline{UB} , \overline{LB} Controlled)



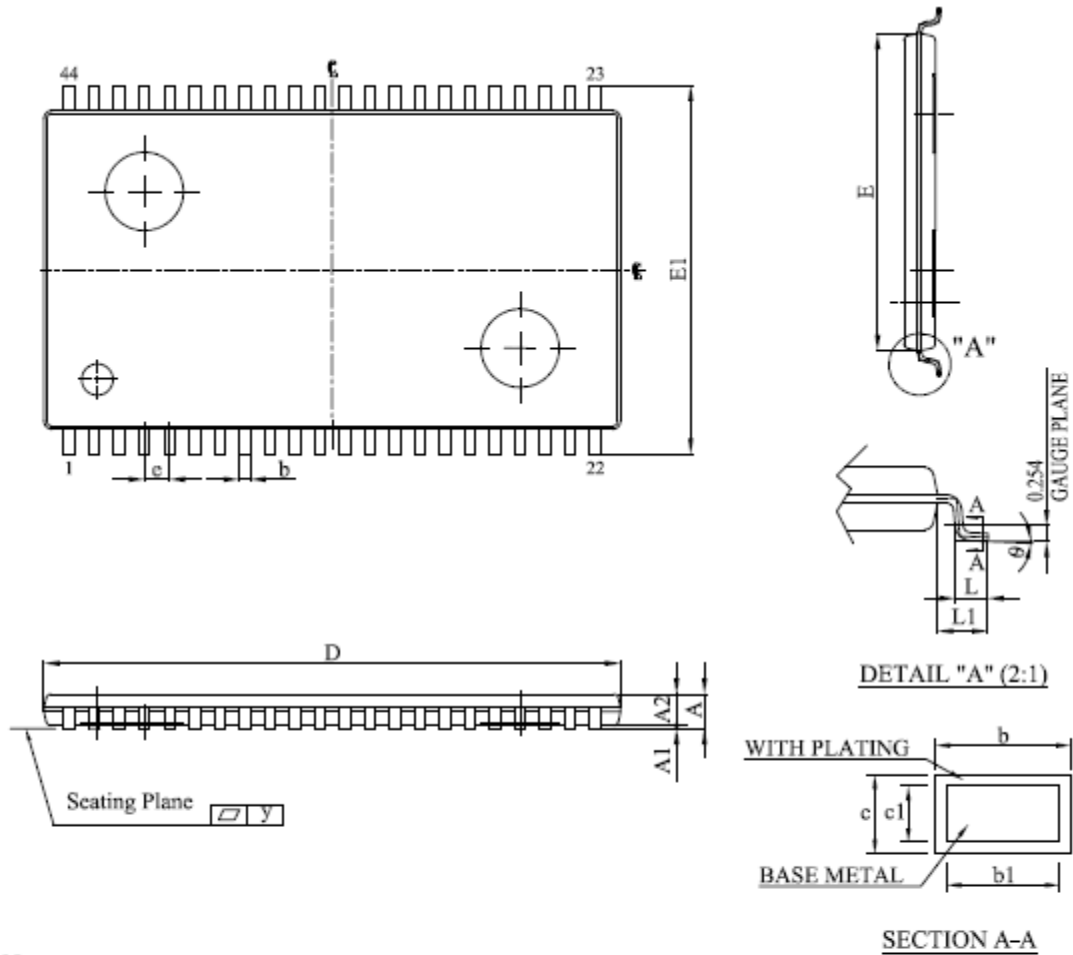
NOTES (Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low ;
A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of \overline{CS} going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. \overline{WE} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.
6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When \overline{CS} is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

** Those parameters are applied for x16 mode only

Package outline dimensions

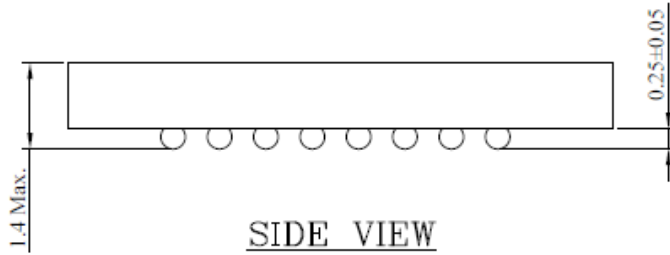
44L-TSOP2-400mil



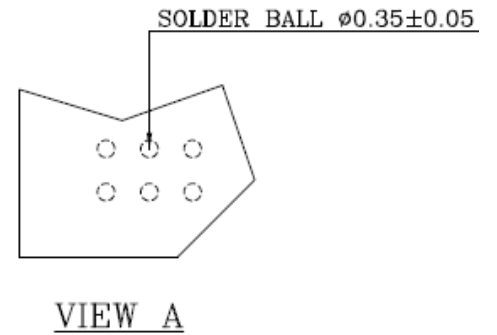
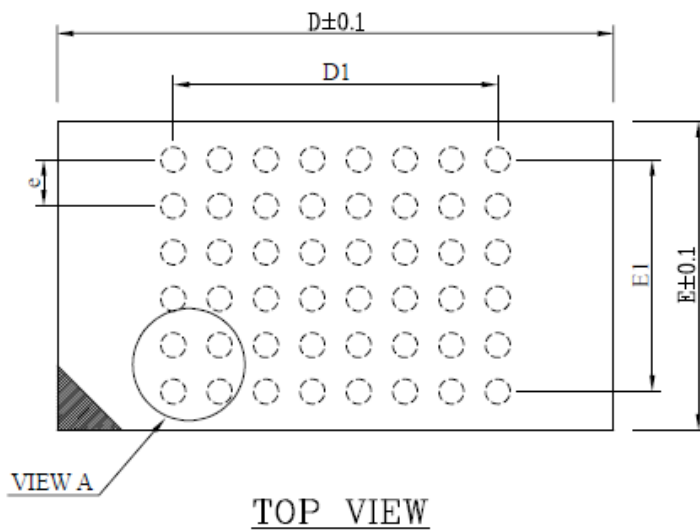
Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

| SYMBOL | | A | A1 | A2 | b | b1 | c | c1 | D | E | E1 | e | L | L1 | y | ⊙ |
|--------|------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|-------|----|
| UNIT | | | | | | | | | | | | | | | | |
| mm | Min. | 1.00 | 0.05 | 0.95 | 0.30 | 0.30 | 0.12 | 0.12 | 18.31 | 10.06 | 11.56 | 0.70 | 0.40 | 0.70 | — | 0° |
| | Nom. | 1.10 | 0.10 | 1.00 | — | — | — | — | 18.41 | 10.16 | 11.76 | 0.80 | 0.50 | 0.80 | — | — |
| | Max. | 1.20 | 0.15 | 1.05 | 0.45 | 0.40 | 0.21 | 0.16 | 18.51 | 10.26 | 11.96 | 0.90 | 0.60 | 0.90 | 0.1 | 8° |
| inch | Min. | 0.0393 | 0.002 | 0.037 | 0.012 | 0.012 | 0.005 | 0.005 | 0.721 | 0.396 | 0.455 | 0.0275 | 0.0157 | 0.0275 | — | 0° |
| | Nom. | 0.0433 | 0.004 | 0.039 | — | — | — | — | 0.725 | 0.400 | 0.463 | 0.0315 | 0.0197 | 0.0315 | — | — |
| | Max. | 0.0473 | 0.006 | 0.041 | 0.018 | 0.016 | 0.008 | 0.006 | 0.729 | 0.404 | 0.471 | 0.0355 | 0.0237 | 0.0355 | 0.004 | 8° |

48ball mini-BGA-6x8mm (ball pitch: 0.75mm)



| BALL PITCH e = 0.75 | | | | |
|---------------------|-----|----|------|------|
| D | E | N | D1 | E1 |
| 8.0 | 6.0 | 48 | 5.25 | 3.75 |



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.