



1M Async Fast SRAM

CS16FS1024(3//W)

Cover Sheet and Revision Status

版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0		Apr.15,2014	New issue	Hank Lin
2.0		May 26, 2014	Delete 128kx8 products	Hank Lin
3.0		May 22, 2015	Add 32TSOPII-400mil pin configuration and outline	Hank Lin
4.0		Jan. 13, 2017	Add part no. CS16FS10245GC(I)-12 in order information	Hank Lin
5.0		Nov. 8, 2021	Revise "Chiplus reserves the right to change product or specification without notice" to "Chiplus reserves the right to	Hank Lin
6.0	20240007	May. 23, 2024	Delete 5V product	Hank Lin



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CS16FS1024(3/W)

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CS16FS1024(3//W)

GENERAL DESCRIPTION

The CS16FS1024(3//W) is a 1,048,576-bit high-speed Static Random Access Memory organized as 64K words by 16 bits. The CS16FS1024(3//W) uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. And CS16FS1024(3//W) allows that lower and upper byte access by data byte control (\overline{UB} , \overline{LB}). The device is fabricated using advanced CMOS process, 6-TR based cell technology and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The CS16FS1024(3//W) is packaged in a 400mil 44-pin TSOP2 and 48FBGA.

FEATURES

- Fast Access Time 8,10,12,15ns(Max)
- CMOS Low Power Dissipation
Standby (TTL): 10mA (Max.)
(CMOS): 6mA (Max.)
Operating: 35mA (8ns, Max..)
: 30mA(10ns ,Max.)
- Single 3.3±0.3V Power Supply
- Wide range (1.65V~3.6V) of Power Supply
- TTL Compatible inputs and Outputs
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control(x16 Mode)
 \overline{LB} : I/O₀~I/O₇, \overline{UB} : I/O₈~I/O₁₅
- Standard 48FBGA and 44TSOP2 Package Pin Configuration for 64K x 16
- Operating in Commercial and Industrial Temperature range



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CS16FS1024(3/W)

Order Information

Density	Org.	Part Number	V _{CC} (V)	Speed		Package	Temp.
				t _{AA} (ns)	t _{OE} (ns)		
1Mb	64Kx16	CS16FS10243GC(I)-08	3.3	8	4	44 TSOP2	C: Commercial I : Industrial
			3.3	8	4	44 TSOP2	
		CS16FS1024WGC(I)-08*	2.5	10	5	44 TSOP2	
			1.8	12	6	44 TSOP2	
		CS16FS10243HC(I)-08	3.3	8	4	48 FBGA	
			3.3	8	4	48 FBGA	
		CS16FS1024WHC(I)-08*	2.5	10	5	48 FBGA	
			1.8	12	6	48 FBGA	
		CS16FS10243GC(I)-10	3.3	10	5	44 TSOP2	
			3.3	10	5	44 TSOP2	
		CS16FS1024WGC(I)-10*	2.5	10	5	44 TSOP2	
			1.8	15	7	44 TSOP2	
		CS16FS10243HC(I)-10	3.3	10	5	48 FBGA	
			3.3	10	5	48 FBGA	
		CS16FS1024WHC(I)-10*	2.5	10	5	48 FBGA	
			1.8	15	7	48 FBGA	

*means max. speed



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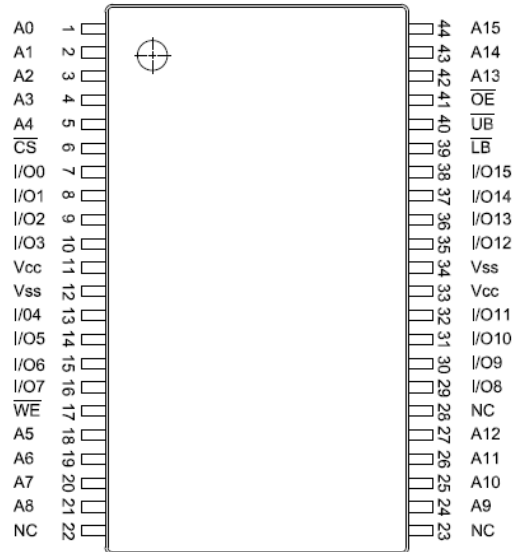
PIN CONFIGURATIONS

48ball mini-BGA

44TSOP2-400mil

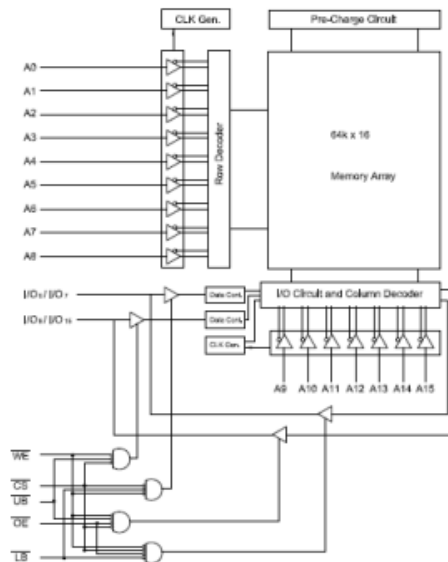
	1	2	3	4	5	6
A	\overline{LB}	\overline{OE}	A0	A1	A2	NC
B	IO8	\overline{UB}	A3	A4	\overline{CS}	IO0
C	IO9	IO10	A5	A6	IO1	IO2
D	Vss	IO11	NC	A7	IO3	Vcc
E	Vcc	IO12	NC	NC	IO4	Vss
F	IO14	IO13	A14	A15	IO5	IO6
G	IO15	NC	A12	A13	WE	IO7
H	NC	A8	A9	A10	A11	NC

CS16FS1024(3/W)- (64k x 16)



CS16FS1024(3/5/W)-(64k x 16)

FUNCTIONAL BLOCK DIAGRAM





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CS16FS1024(3//W)

Absolute Maximum Ratings*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	3.3V Product	V _{in} , V _{OUT}	-0.5 to V _{CC} +0.5V	V
	Wide V _{CC} ** Product			
Voltage on V _{CC} Supply Relative to V _{SS}	3.3V Product	V _{in} , V _{OUT}	-0.5 to 4.0	V
	Wide V _{CC} ** Product		-0.5 to 4.0	
Power Dissipation		P _D	1.0	W
Storage Temperature		T _{STG}	-65 to 150	°C
Operating Temperature Commercial		T _A	0 to 70	°C
Industrial		T _A	-40 to 85	°C

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Wide VCC Range is 1.65V~3.6V

Recommended DC Operating Conditions*(T_A=0 to 70°C)

Parameter	Operating V _{CC} (V)	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	3.3	V _{CC}	3.0	3.3	3.6	V
	Wide 2.4~3.6	V _{CC}	2.4	2.5/3.3	3.6	
	Wide 1.65~2.2	V _{CC}	1.65	1.8	2.2	
Ground		V _{SS}	0	0	0	V
Input High Voltage	3.3	V _{IH}	2.0	-	V _{CC} +0.5	
	Wide 2.4~3.6	V _{IH}	2.0	-	V _{CC} +0.3	
	Wide 1.65~2.2	V _{IH}	1.4	-	V _{CC} +0.2	
Input Low Voltage	3.3	V _{IL}	-0.3	-	0.8	V
	Wide 2.4~3.6	V _{IL}	-0.3	-	0.7	
	Wide 1.65~2.2	V _{IL}	-0.2	-	0.4	

*The above parameters are also guaranteed for industrial temperature range.



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CS16FS1024(3/W)

DC and Operating Characteristics*(T_A=0 to 70°C)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-2	2	uA	
Output Leakage Current**	I _{LO}	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{OUT} =V _{SS} to V _{CC}	-2	2	uA	
Operating Current**	I _{CC}	Min.Cycle, 100% Duty $\overline{CS} = V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} = 0mA	8ns	-	32	mA
			10ns	-	30	
			12ns	-	28	
			15ns	-	25	
Standby Current	I _{SB}	Min. Cycle, $\overline{CS} = V_{IH}$	-	15	mA	
	I _{SB1}	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$ V _{IN} ≥V _{CC} -0.2V or V _{in} ≤0.2V	-	9		
Output Low Voltage Level	V _{OL}	V _{CC} =3.0V, I _{OL} =8mA, 3.3V Product & Wide V _{CC} ** Product	-	0.4	V	
		V _{CC} =2.4V, I _{OL} =1mA, Wide V _{CC} ** Product	-	0.4		
		V _{CC} =1.65V, I _{OL} =0.1mA, Wide V _{CC} ** Product	-	0.2		
Output High Voltage Level	V _{OH}	V _{CC} =3.0V, I _{OH} = -4mA, 3.3V Product & Wide V _{CC} ** Product	2.4	-	V	
		V _{CC} =2.4V, I _{OH} = -1mA, Wide V _{CC} ** Product	1.8	-		
		V _{CC} =1.65V, I _{OH} = -0.1mA, Wide V _{CC} ** Product	1.4	-		

*The above parameters are also guarantee for industrial temperature range.

**Wide V_{CC} Range is 1.65V ~ 3.6V



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Capacitance*($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

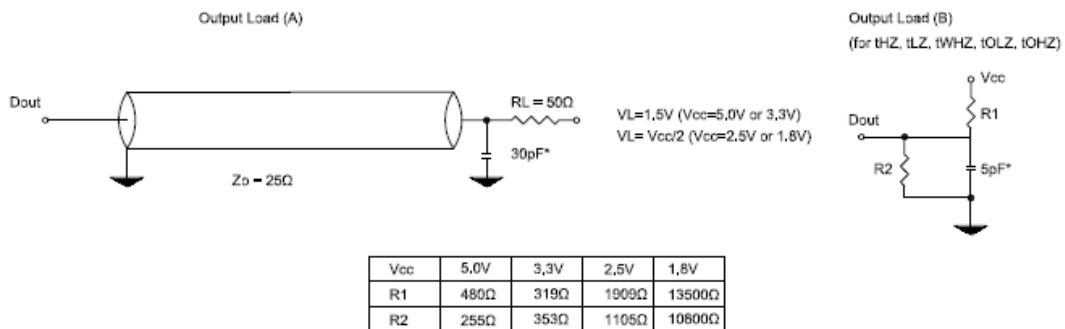
Item	Symbol	Test Conditions	TYP	Max	Unit
Input/ Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	-	8	pF
Input Capacitance	C_{IN}	$V_{IN}=0\text{V}$	-	6	pF

*Capacitance is sampled and not 100% tested.

Test Conditions*

Parameter	Value
Input/ Output Capacitance	0 to 3.0V ($V_{CC}=3.3\text{V}$)
	0 to 2.5V ($V_{CC}=2.5\text{V}$)
	0 to 1.8V ($V_{CC}=1.8\text{V}$)
Input Rise and Fall Time	1V/1ns
Input and Output Timing Reference Levels	1.5V ($V_{CC}=3.3\text{V}$)
	1/2 V_{CC} ($V_{CC}=1.8\text{V}$ or 2.5V)
Output Load	See Fig. 1

*The above parameters are also guaranteed for industrial temperature range.



* Including Scope and Jlg Capacitance

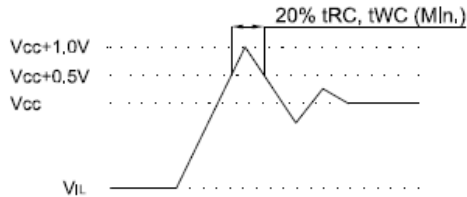
Fig 1



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CS16FS1024(3/W)

Overshoot Timing



Undershoot Timing

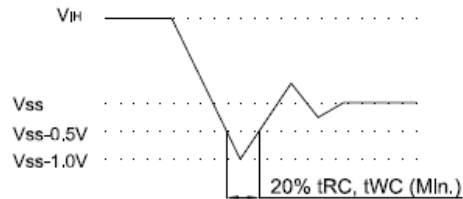


Fig 2

Functional Description (x8 Mode)

\overline{CS}	\overline{WE}	\overline{OE}	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D _{OUT}	I_{CC}
L	L	X	Write	D _{IN}	I_{CC}

*X means don't care

Functional Description (x16 Mode)

\overline{CS}	\overline{WE}	\overline{OE}	\overline{LB}^{**}	\overline{UB}^{**}	Mode	I/O Pin		Supply Current
						I/O ₀ ~I/O ₇	I/O ₈ ~I/O ₁₅	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D _{OUT}	High-Z	I_{CC}
			H	L		High-Z	D _{OUT}	
			L	L		D _{OUT}	D _{OUT}	
L	L	X	L	H	Write	D _{IN}	High-Z	I_{CC}
			H	L		High-Z	D _{IN}	
			L	L		D _{IN}	D _{IN}	



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*X means don't care

Data Retention Characteristics*(T_A=0 to 70°C)

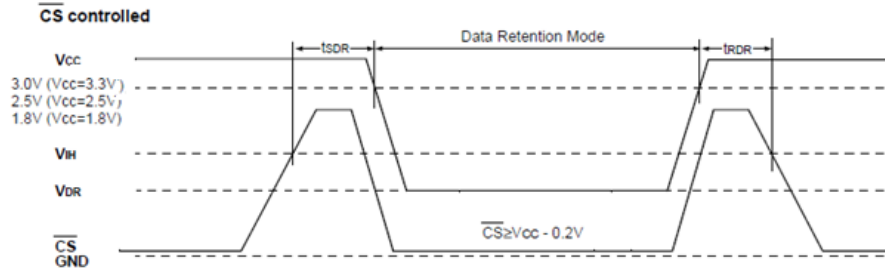
Parameter	Product	Operating V _{CC} (V)	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V _{CC} for Data Retention	3.3V Product	3.3	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	3.6	V
	Wide 2.4V~3.6V	2.5/3.3			2.0	-	3.6	
	Wide 1.65V~2.2V	1.8			1.5	-	3.6	
Data Retention Current	3.3V Product	3.3	I _{DR}	V _{CC} =2.0V $\overline{CS} \geq V_{CC} - 0.2V$	-	-	5	mA
	Wide 2.4V~3.6V	2.5/3.3		V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	-	-	6	
	Wide 1.65V~2.2V	1.8		V _{CC} =1.5V, $\overline{CS} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	-	-	6	
Data Retention Set-Up Time			t _{SDR}	See Data	0	-	-	nS
Recovery Time			t _{RDR}	Retention Wave form (below)	5	-	-	mS



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Data Retention Wave form



Read Cycle*

Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	8	-	10	-	12	-	15	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	-	7	ns
$\overline{UB}, \overline{LB}$ Access Time**	t_{BA}	-	4	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
$\overline{UB}, \overline{LB}$ Enable to Low-Z Output**	t_{BLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	0	7	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	0	7	ns
$\overline{UB}, \overline{LB}$ Disable to High-Z	t_{BHZ}	0	4	0	5	0	6	0	7	ns

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Output**										
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection Power Up Time	t _{PU}	0	-	0	-	0	-	0	-	ns
Chip Selection Power Down Time	t _{PD}	-	8	-	10	-	12	-	15	ns

*The above parameters are also guaranteed for industrial temperature range.

Write Cycle*

Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	8	-	10	-	12	-	15	-	ns
Chip Select to End of Write	t _{CW}	6	-	7	-	9	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	6	-	7	-	9	-	12	-	ns
Write Pulse Width(\overline{OE} High)	t _{WP}	6	-	7	-	9	-	12	-	ns
Write Pulse Width(\overline{OE} Low)	t _{WP1}	8	-	10	-	12	-	15	-	ns
\overline{UB} , \overline{LB} Valid to End of Write**	t _{BW}	6	-	7	-	9	-	12	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	4	0	5	0	6	0	7	ns
Data to Write Time Overlap	t _{DW}	4	-	5	-	7	-	8	-	ns
Data Hold from Write	t _{DH}	0	-	0	-	0	-	0	-	ns



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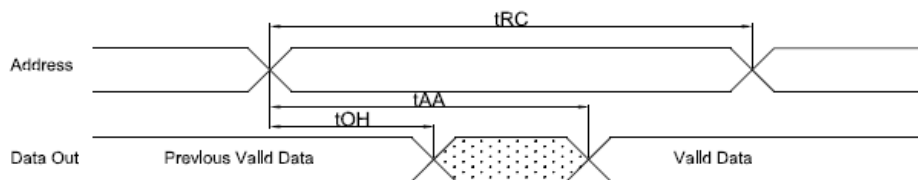
CS16FS1024(3/W)

Time										
End of Write to Output Low-Z	t_{ow}	3	-	3	-	3	-	3	-	ns

*The above parameters are also guaranteed for industrial temperature range.

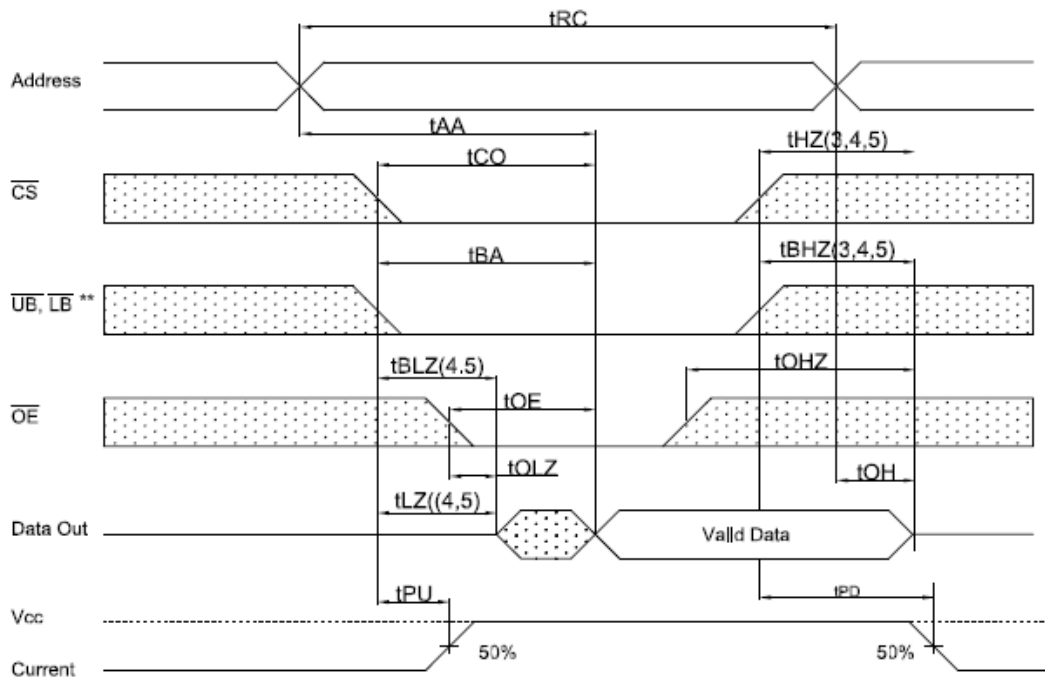
Timing Diagram

Timing Waveform of Read Cycle (1) (Address Controlled, $\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, \overline{UB} , $\overline{LB} = V_{IL}$ **)



** Those parameters are applied for x16 mode only.

Timing Waveform of Read Cycle (2) ($\overline{WE} = V_{IH}$)





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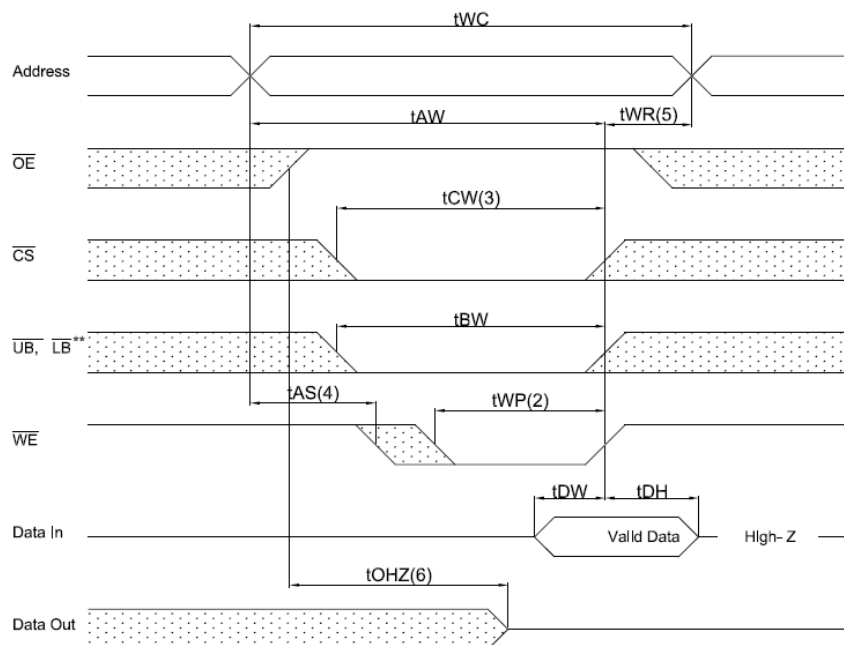
CS16FS1024(3/W)

NOTES (Read Cycle)

1. \overline{WE} is high for read cycle
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS} = V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (1) (\overline{OE} Clock)



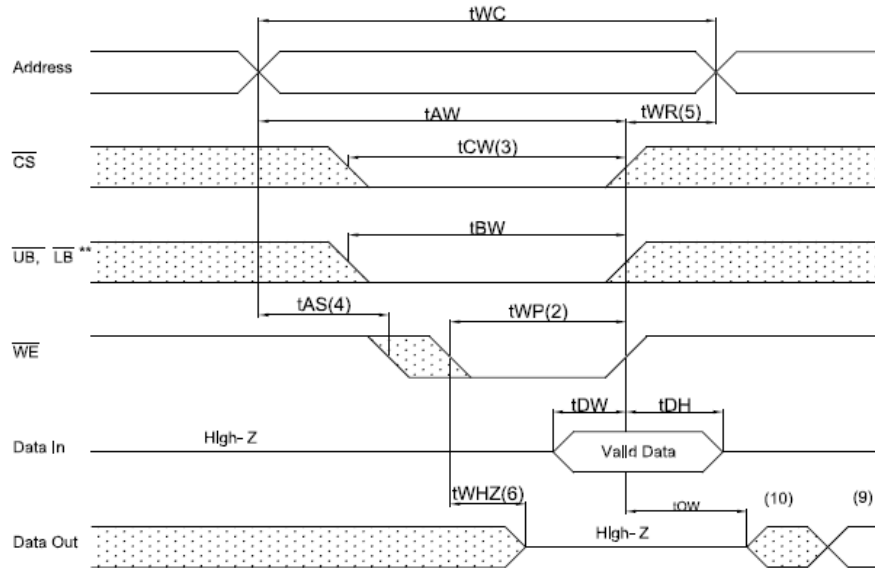
** Those parameters are applied for x16 mode only.



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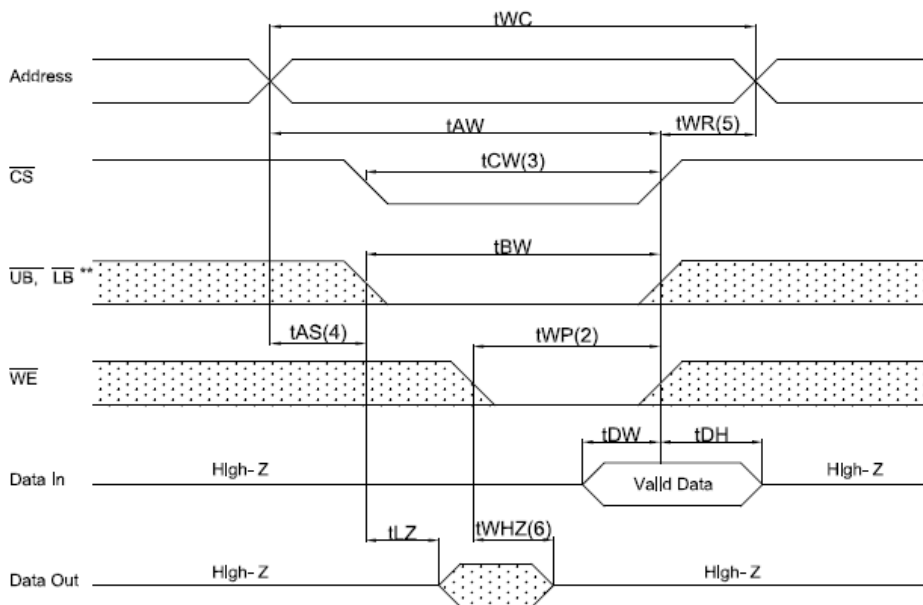
CS16FS1024(3/W)

Timing Waveform of Write Cycle (2) (\overline{OE} = Low fixed)



** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (3) (\overline{CS} = Controlled)



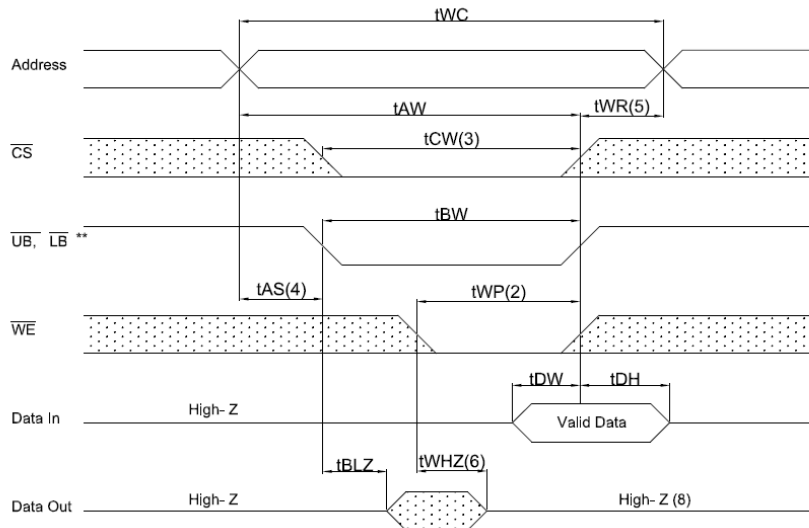
** Those parameters are applied for x16 mode only.



1M Async Fast SRAM

CS16FS1024(3/W)

Timing Waveform of Write Cycle (4) (\overline{UB} , \overline{LB} Controlled)



NOTES (Write Cycle)

- All write cycle timing is referenced from the last valid address to the first transition address.
- A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low ;
A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
- t_{CW} is measured from the later of \overline{CS} going low to end of write.
- t_{AS} is measured from the address valid to the beginning of write.
- \overline{WE} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.
- If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
- D_{OUT} is the read data of the new address.
- When \overline{CS} is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

** Those parameters are applied for x16 mode only

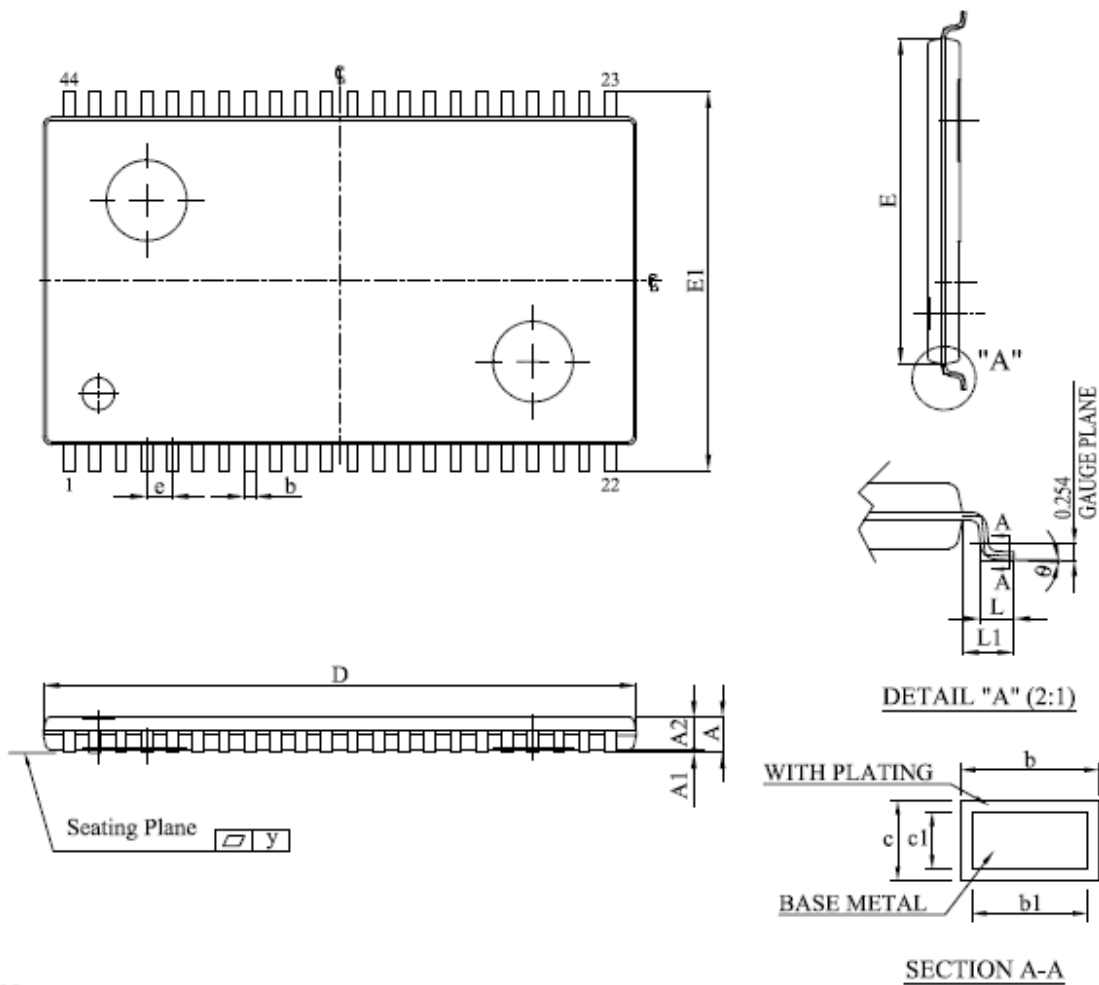


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CS16FS1024(3/W)

Package outline dimensions

44L-TSOP2-400mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

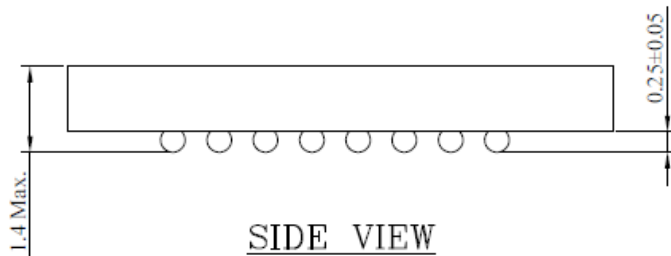
SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ
UNIT																
mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	-	0°
	Nom.	1.10	0.10	1.00	-	-	-	-	18.41	10.16	11.76	0.80	0.50	0.80	-	-
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	-	-	-	-	0.725	0.400	0.463	0.0315	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°



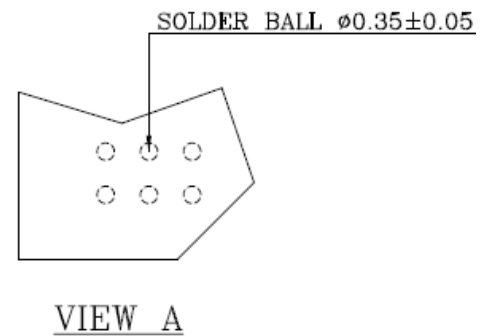
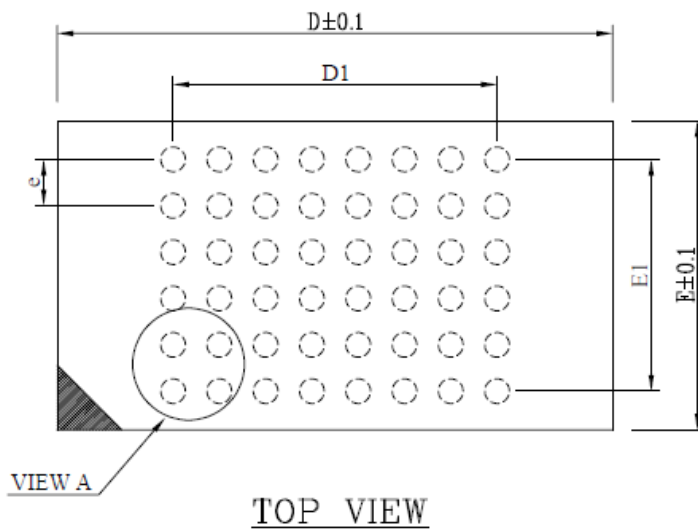
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CS16FS1024(3/W)

48ball mini-BGA-6x8mm (ball pitch: 0.75mm)



BALL PITCH $e = 0.75$				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.