Cover Sheet and Revision Status

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CS8364xx

64Mb SPI/QPI PSRAM

General Description

The 64Mb QSPI PSRAM (Pseudo Static RAM) is a low power, high-speed CMOS Double Data Rate, self- refresh DRAM with a low pin count Quad-SPI interface.
The dynamic cell in the DRAM array needs to be refreshed periodically. Internal refresh control logic of PSRAM manages the refresh operation of array cell when the memory isn't actively engaged for reading or writing by the host. Since the host is not required to manage any refresh operations, the DRAM array seems to the host as if it employs static cells capable of retaining data without the need for refresh. Therefore, the memory is described as Pseudo Static RAM (PSRAM).
QSPI PSRAM connects to a host system via a serial peripheral interface (SPI). SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional four bits wide Quad I/O (QIO) and Quad Peripheral Interface (QPI) commands.

Features

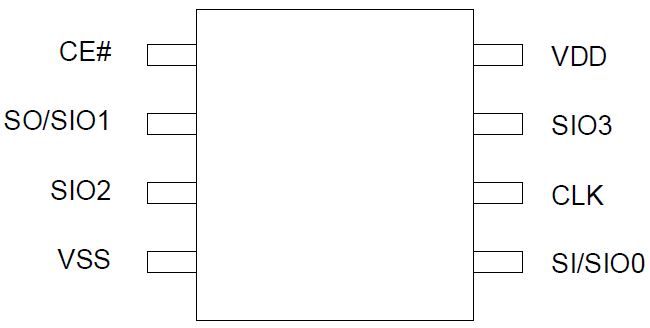
- Interface and Power Supply
  - SPI/QPI with SDR mode
  - VDD=1.62~1.98V / 2.7~3.6V
  - Output driver LVCMOS
  - 50Ω output drive strength
- Performance: Clock rate up to
  - 143MHz for 32 Bytes Wrapped Burst
  - 84MHz for Linear Burst operation with row boundary crossing
- Organization
  - 64Mb, 8M x 8bits
  - 1024 bytes page size
  - Addressable Bit Range: A[22:0]
- Self-managed refresh
- Power Saving Modes
  - Auto temperature compensated self-refresh by built-in temperature sensor
  - Ultra low power hybrid sleep mode
- Linear Burst (continuous) or 32 bytes wrapped burst via toggle command.
- Linear Burst can cross page boundary as long as tCEM is met and is supported up to 84MHz.
- Software Reset

Order Information

Part No.	Mode	VDD	Max Clock	Temperature Range	Package
CS836411NP-7	SPI	1.62V~1.98V	143 MHz	-40°C to 85°C	SOP-8L
CS836441NP-7	QPI				
CS836413NP-7	SPI	2.7V~3.6V			
CS836443NP-7	QPI				

Pin Configurations

8L SOP-150mil



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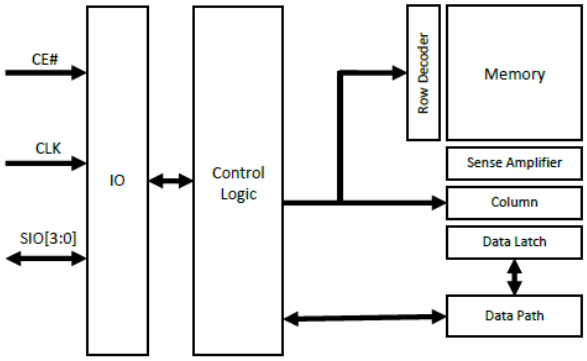
Pin Descriptions

Symbol	Type	Function
CE#	Input	Chip Select: CE# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CE# is sampled HIGH.
CLK	Input	Clock: CLK is driven by the system clock. All inputs to this device are acquired in synchronization with the rising edge of this pin.
SI/SIO0	I/O	Serial Input in single bit data commands or IO0 in Quad mode.
SO/SIO1	I/O	Serial Output in single bit data commands or IO1 in Quad mode.
SIO2	I/O	IO2 in Quad mode
SIO3	I/O	IO3 in Quad mode
VDD	Power Supply	Power Supply
VSS	Power Supply	Ground

Logic Block Diagram



Note 1: This Logic Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Power-Up Initialization

Prior to normal operation, the PSRAM must be initialized. The SPI/QPI PSRAM device include an on-chip voltage sensor used to launch the power-up initialization process. When the power supply reaches a stable level at or above minimum VDD, the device will require 150µs and software reset operation to complete its self-initialization process.

The device must not be selected during power-up. CE# must follow the voltage applied on VDD until VDDmin is reached (track VDD within 200mV) and then CE# remain high for a further 150µs, CLK and SI/SO/SIO3:0 must remain low.
After the 150µs period of device initialization and a subsequent software reset operation (tRST≧50ns), the device is ready for normal operation.

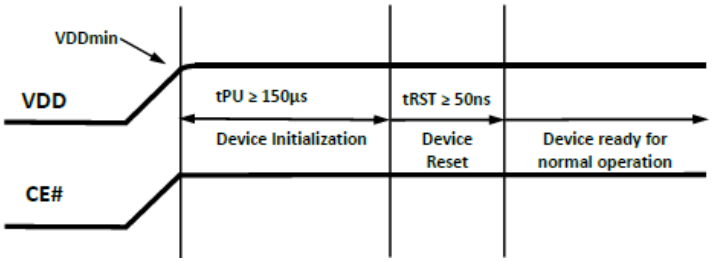


Figure 1. Power-Up Initialization Timing

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Interface Description

Address Space

SPI/QPI PSRAM device is byte-addressable. 64M device is addressed with A[22:0].

Page Size and Burst Length

Page size is 1K Bytes (CA[9:0]). Default burst setting is Linear Bursting that crosses page boundary in a continuous manner. Note however that burst operations which cross page boundary have a lower max input clock frequency of 84MHz, and it can cross page boundary one time only in a burst.
The wrap 32 can also be set by Wrap Boundary Toggle command and there is no page boundary crossing function supported in this configuration.

Drive Strength

The device powers up in 50Ω.

Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

Command/Address Latching Truth Table

The device recognizes the following commands specified by the various input methods.

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Addr	Wait Cycle	DIO	Max Freq	Cmd	Addr	Wait Cycle	DIO	Max Freq
Read	‘h03	S	S	0	S	33	NA				
Fast Read	‘h0B	S	S	8	S	143/84*	Q	Q	4	Q	66
Fast Read Quad	‘hEB	S	Q	6	Q	143/84*	Q	Q	6	Q	143/84*
Write	‘h02	S	S	0	S	143/84*	Q	Q	0	Q	143/84*
Quad Write	‘h38	S	Q	0	Q	143/84*	Q	Q	0	Q	143/84*
Enter Quad Mode	‘h35	S	-	-	-	143	NA				
Exit Quad mode	‘hF5	NA					Q	-	-	-	143
Reset Enable	‘h66	S	-	-	-	143	Q	-	-	-	143
Reset	‘h99	S	-	-	-	143	Q	-	-	-	143
Wrap Boundary Toggle	‘hC0	S	-	-	-	143	Q	-	-	-	143
Hybrid Sleep Entry	‘hC1	S	-	-	-	143	Q	-	-	-	143
Read ID	‘h9F	S	S	0	S	33	NA				

Remark : S = Serial IO, Q = Quad IO

**Note: 144MHz is maximum clock frequency under Warp 32 operation; 84MHz is maximum clock frequency under Linear Burst operation with page boundary crossing access.*

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Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active command and set the device into standby. Not doing so will block internal refresh operations and leads to memory failure.

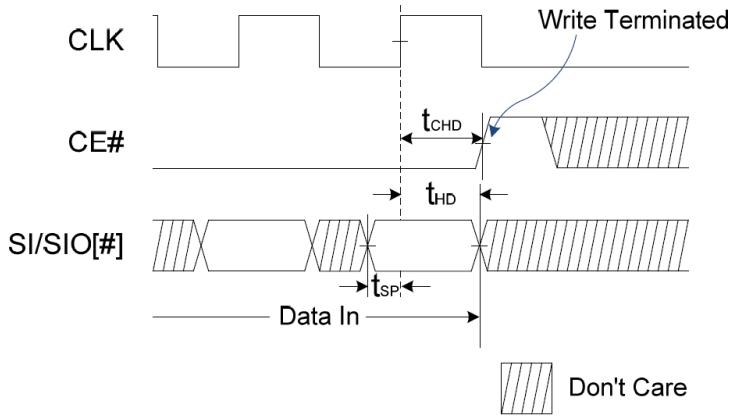

Figure 2: Write Command Termination

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time (tCHD > tACLK+tCLK) for a sufficient data window.

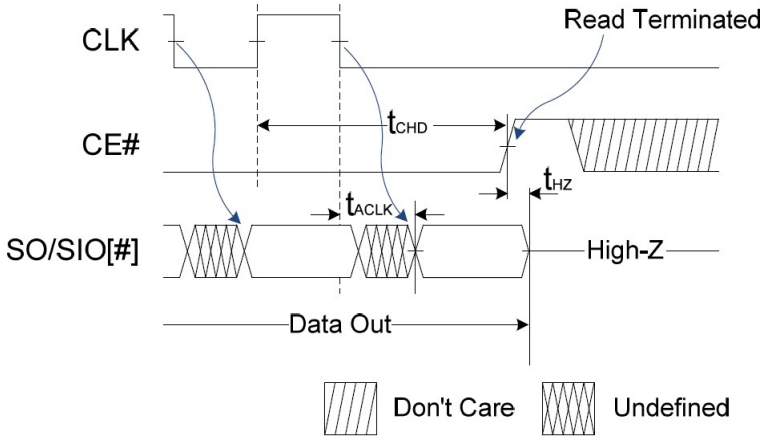

Figure 3: Read Command Termination

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Wrap Boundary Toggle Operation

The Wrap Boundary Toggle Operation switches the device's wrapped boundary between Linear Burst which crosses the 1K page boundary (CA[9:0]) and wrap 32 (CA[4:0]) bytes. Default setting is Linear Burst.

Linear Burst allows the device to burst through page boundary. Page boundary crossing is invisible to the memory controller and limited to a lower max CLK frequency of 84MHz.

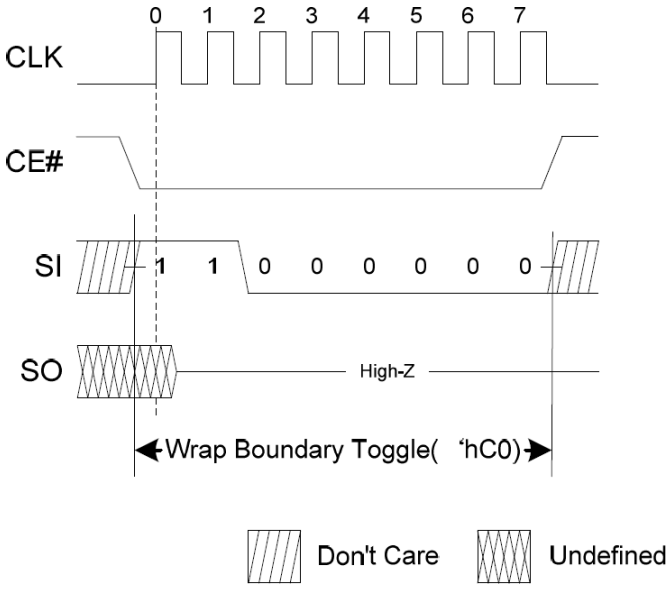

Figure 4: SPI Wrap Boundary Toggle 'hC0

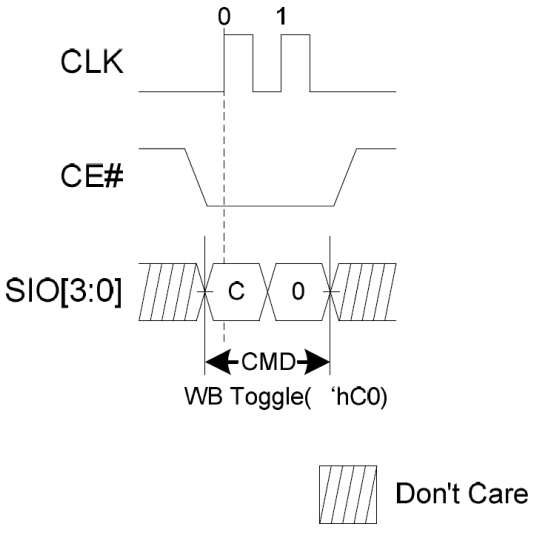

Figure 5: QPI Wrap Boundary Toggle 'hC

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Hybrid Sleep Mode Operation

Hybrid Sleep Mode is a feature which puts the device in an ultra-low power state, while the stored data is retained. Hybrid Sleep Mode Entry can be entered by issuing a command 'hC1 in SPI. CE# going high initiates the Hybrid Sleep mode and must be maintained for the minimum duration of tHS. The Hybrid Sleep Entry command sequences are shown below.

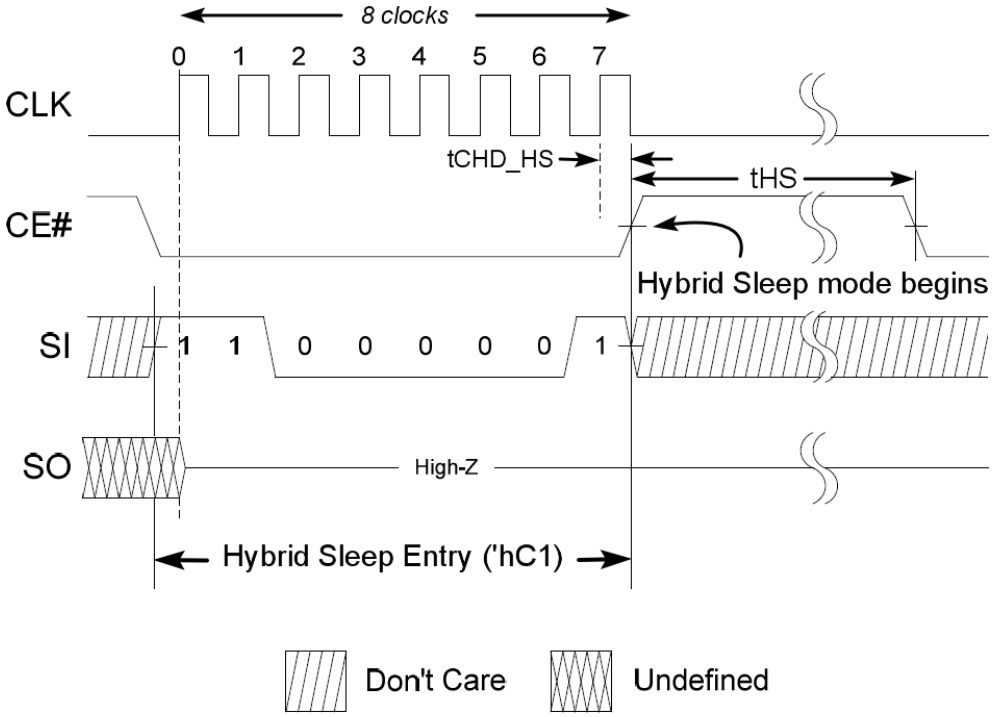

Figure 6: SPI Hybrid Sleep Entry 'hC1

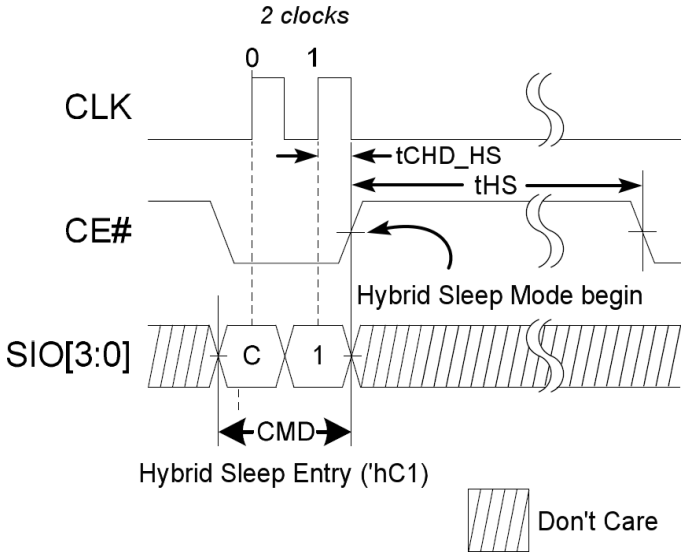

Figure 7: QPI Hybrid Sleep Entry 'hC1

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A low pulsed CE # initiates Hybrid Sleep Exit. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum tXHS)..

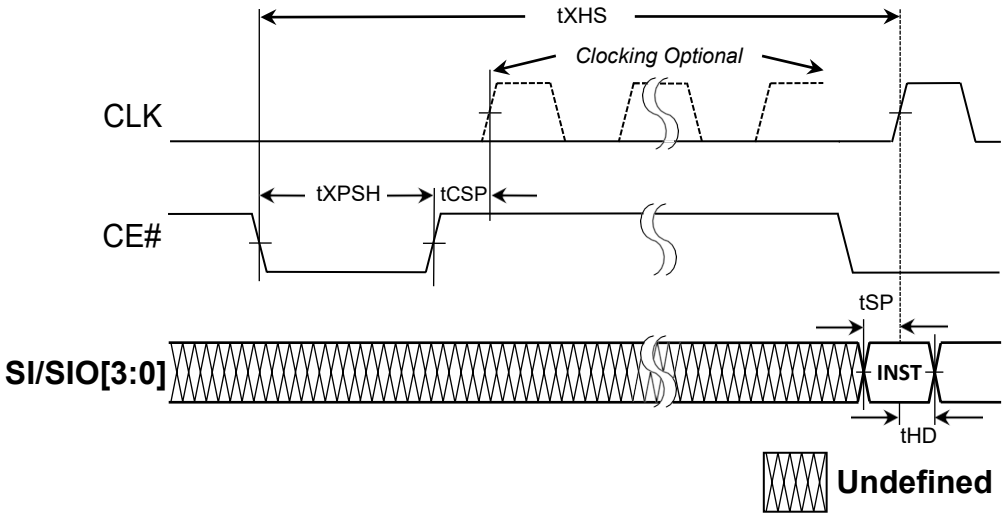

Figure 8: Hybrid Sleep Exit

SPI Mode Operations

The device powers up into SPI mode by default but can also be switched into QPI mode.

SPI Read Operations

For all reads, data will be available tACLK after the falling edge of CLK.

SPI Reads can be done in three ways with Linear Burst or 32 Bytes Wrapped Burst:

1. ‘h03: Serial CMD, Serial Addr/IO, slow frequency,
2. ‘h0B: Serial CMD, Serial Addr/IO, fast frequency
3. ‘hEB: Serial CMD, Quad Addr/IO, fast frequency

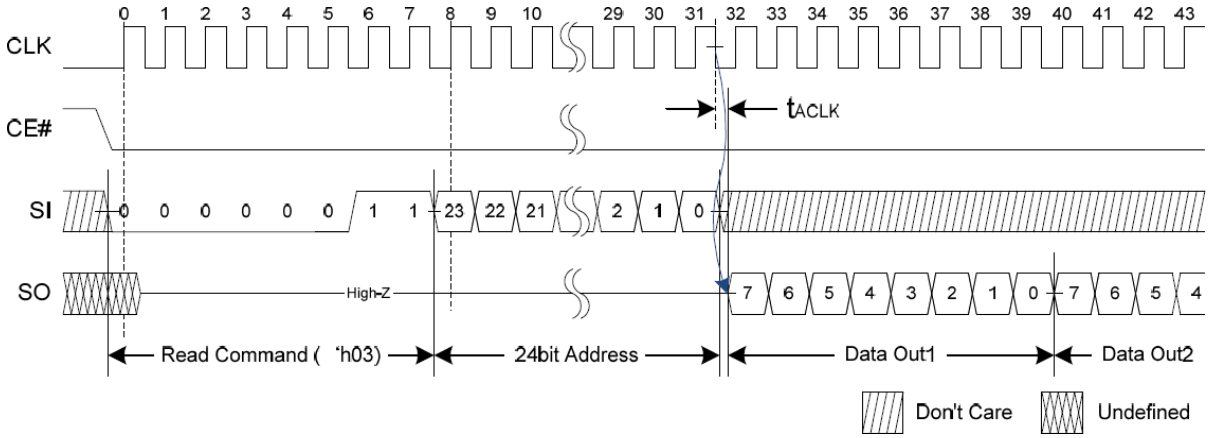

Figure 9: SPI Read ‘h03 (max freq 33MHz)

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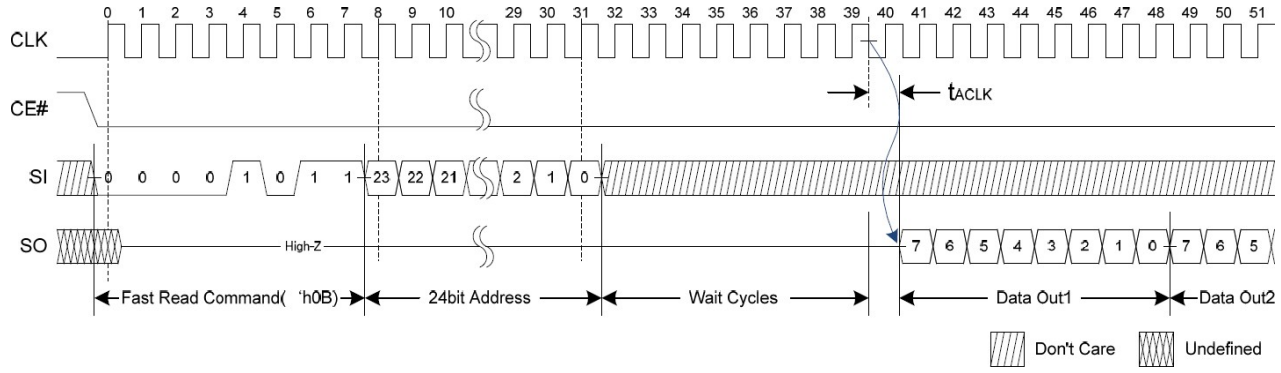

Figure 10: SPI Fast Read 'h0B (max freq 144 MHz)

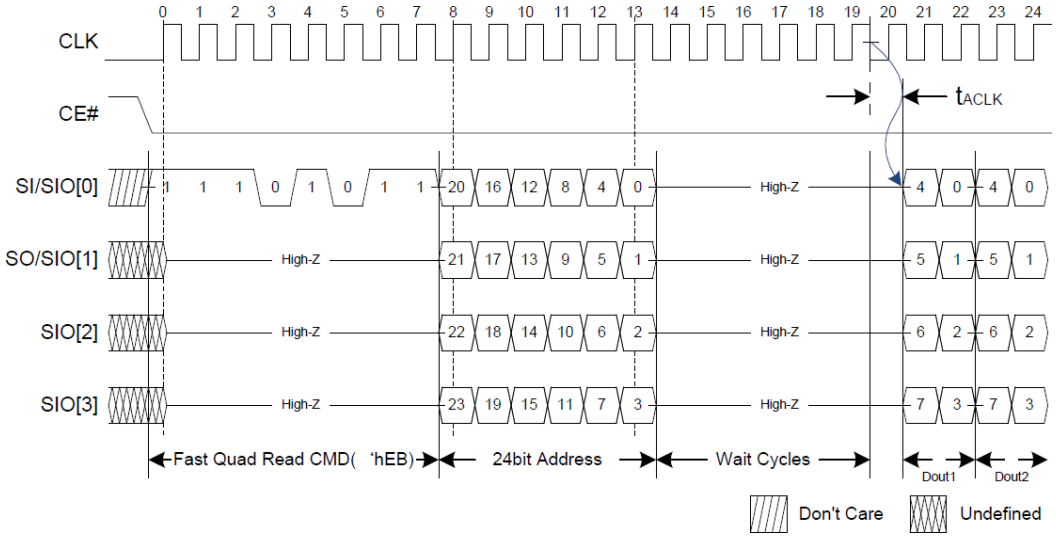

Figure 11: SPI Fast Quad Read 'hEB (max freq 144 MHz)

SPI Write Operations

SPI write command can be input as SPI Write 'h02 or SPI Quad Write 'h38.

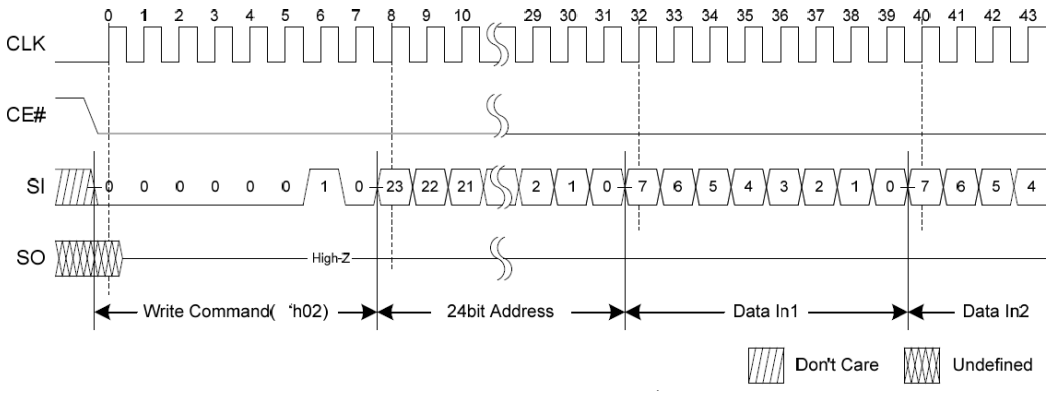

Figure 12: SPI Write 'h02

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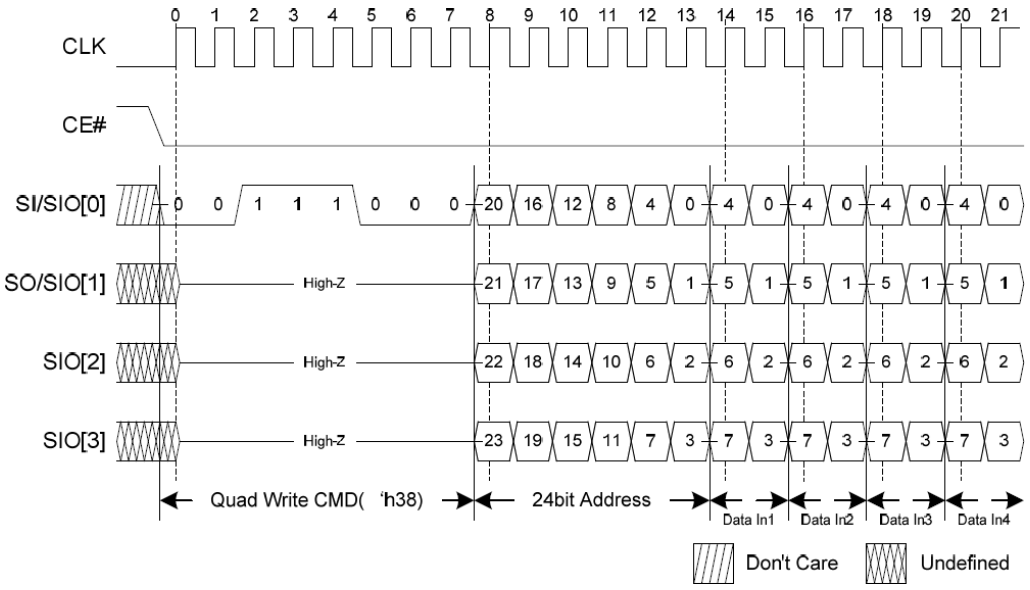

Figure 13: SPI Quad Write 'h38

SPI to QPI Mode Enable Operation

This command switches the device into QPI (quad IO) mode.

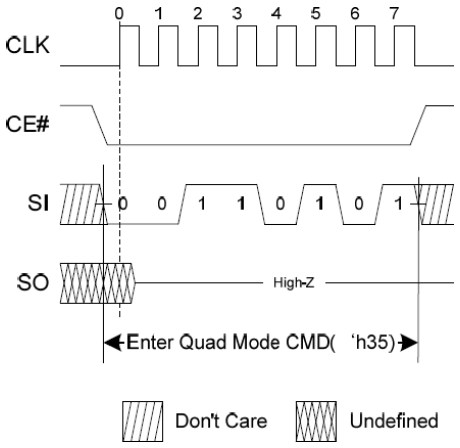

Figure 14: Quad Mode Enable 'h35 (available only in SPI mode)

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Read ID

Read ID command provides information of vendor ID, known-good-die, device density, and manufacturing ID. Note that Read ID command can be used only as Power up initialization after the device Reset tRST≧ 50ns right after Global Reset command.

Figure 15: Pre-condition of EID Read

SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

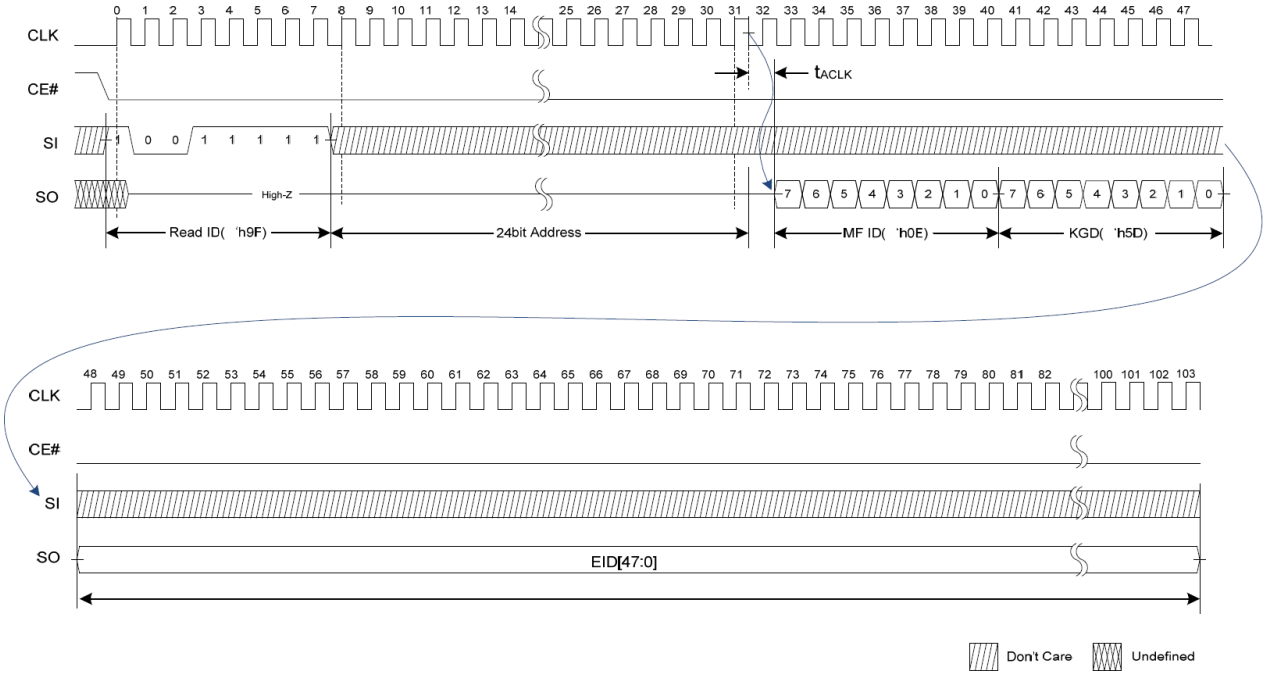

Figure 16: SPI Read ID 'h9F (available only in SPI mode)

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QPI Mode Operations

QPI Read Operation

For all reads, data will be available tACLK after the falling edge of CLK.

QPI Reads can be done in one of two ways with Linear Burst or 32 Bytes Wrapped Burst:
‘

1. h0B: Quad CMD, Quad Addr/IO, slow frequency
2. hEB: Quad CMD, Quad Addr/IO, fast frequency

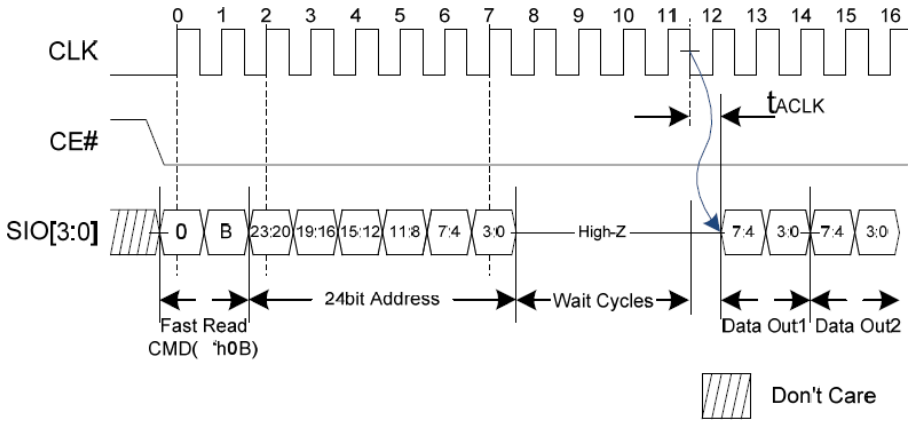

Figure 17: QPI Fast Read ‘h0B (max freq 66 MHz)

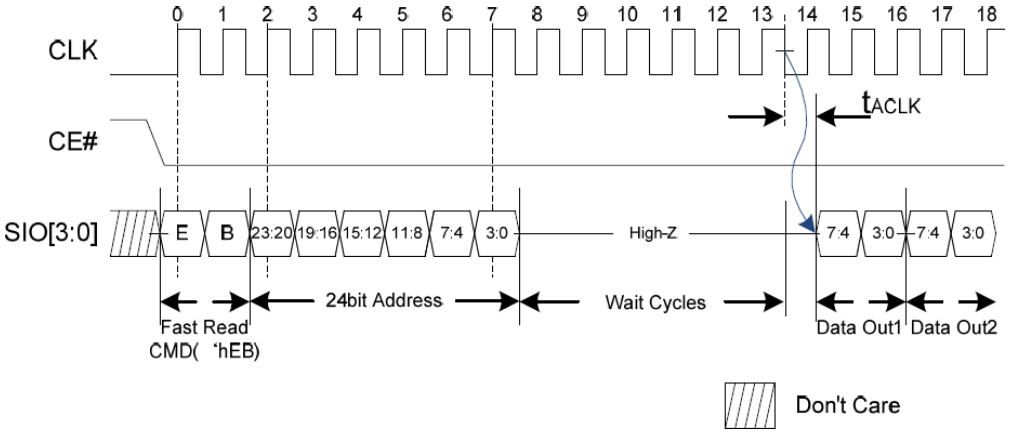

Figure 18: QPI Fast Quad Read ‘hEB (max freq 144 MHz)

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QPI Write Operations

QPI write command can be input as ‘h02 or ‘h38.

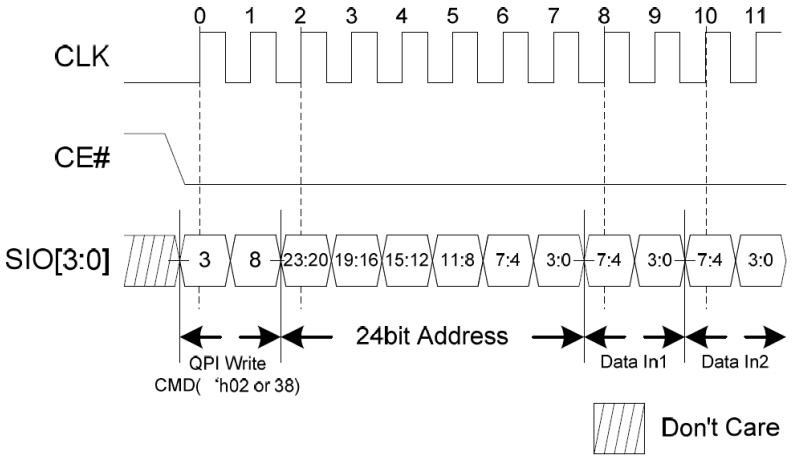

Figure 19: QPI Write ‘h02 or ‘h38

QPI Quad Mode Exit operation

This command will switch the device back into SPI (serial IO) mode.

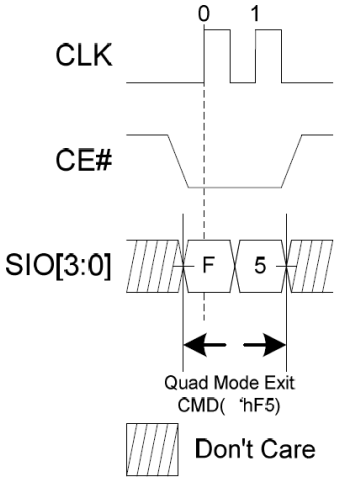

Figure 20: Quad Mode Exit ‘hF5 (only available in QPI mode)

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Reset Operation

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power-up. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

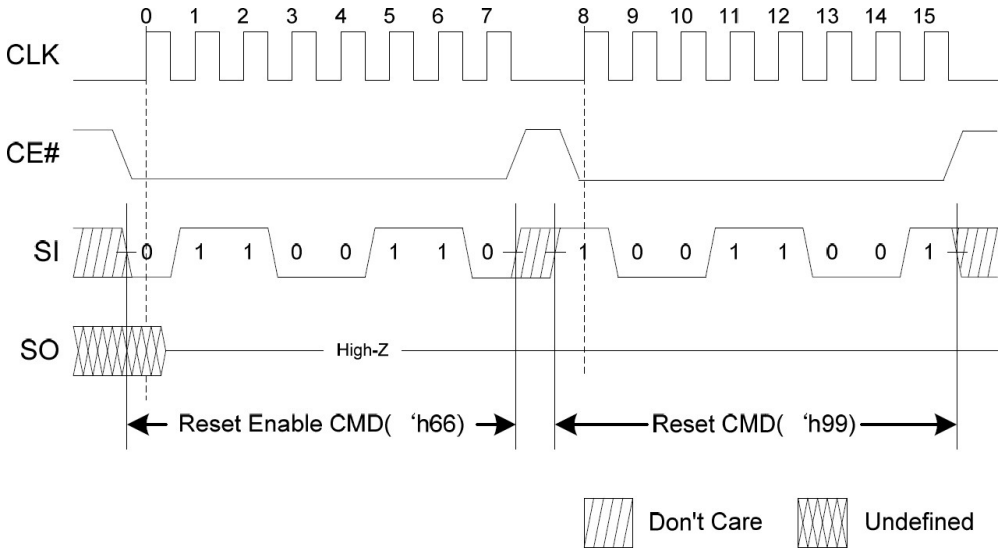

Figure 21: SPI Reset

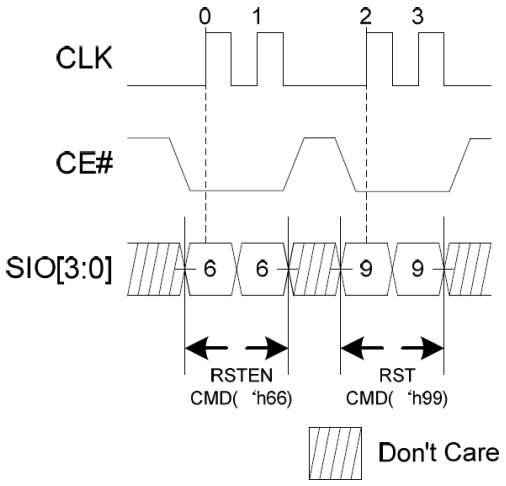

Figure 22: QPI Reset

Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

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Input/Output Timing

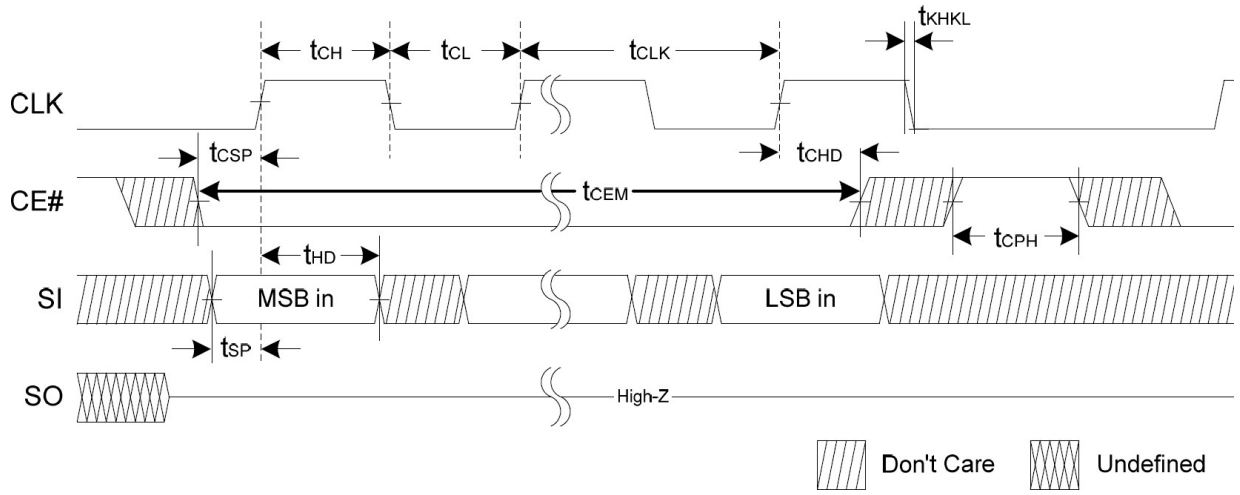

Figure 23: Input Timing

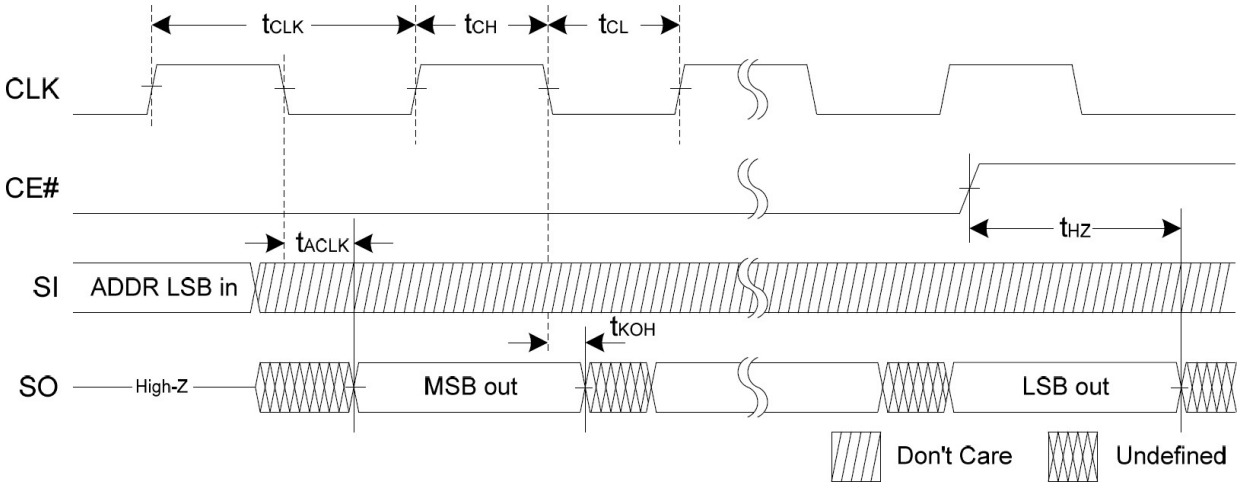

Figure 24: Output Timing

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Electrical Specification

Absolute Maximum Ratings

Absolute Maximum Ratings

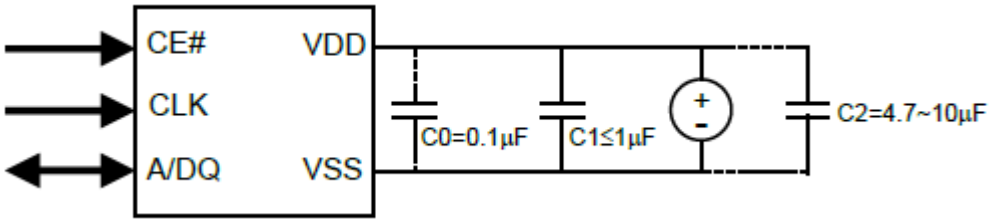
Parameter	Symbol	Rating	Unit
Voltage to any pin except VDD relative to VSS	VT	-0.4 to VDD+0.4	V
Voltage on VDD supply relative to VSS	VDD	-0.4 to +2.45	V
Storage Temperature	TSTG	-55 to +150	°C

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



Low ESR cap C1

It is recommended to place a low ESR decoupling capacitor of <=1µF close to the device to absorb transient peaks. An optional 0.1µF can further improve high frequency transient response.

Large cap C2

During Hybrid sleep modes even though half-sleep average currents are very small (less than 100µA), device will internally have low duty cycle burst refresh for an extended period of time of a few tens of microseconds. These refresh current peaks are large. During this period if the system regulator cannot supply large peaks for several microseconds, it is important to place a 4.7µF-10µF cap to take care of burst refresh currents and replenish the charge before next burst of refreshes.

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DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{DD}	Supply voltage @ 1.8V	1.62	1.98	V	
V_{DD}	Supply voltage @ 3V	2.7	3.6	V	
V_{IH}	Input high leakage	V_{DD}-0.4	V_{DD}+0.2	V	
V_{IL}	Input low leakage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DD}	-	V	
V_{OL}	Output high voltage (I_{OL}=+0.2mA)	-	0.2 V_{DD}	V	
I_{LI}	Input leakage current	-	TBD	μA	
I_{LO}	Output leakage current	-	TBD	μA	
ICC	Read/Write	-	TBD	mA	
ISB_{STD}	Standby current (85°C)	-	TBD	μA	
ISB_{EXT}	Standby current (105°C)		TBD	uA	

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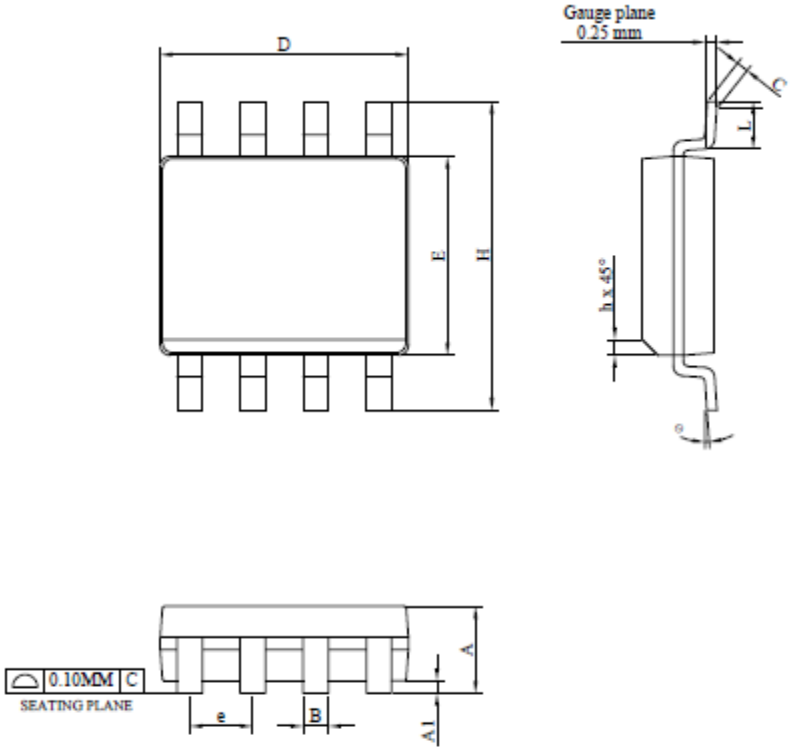
AC Characteristics

Symbol	Parameter		Min	Max	Unit	Note
tCK	Clock period – SPI Read (‘h03)		30.3	-	ns	33 MHz
	Clock period – QPI Read (‘h08)		15.1	-		66 MHz
	Clock period – all other operations with page boundary crossing		11.9	-		84 MHz
	Clock period – all other operations without page boundary crossing		7	-		143 MHz
tCH/tCL	Clock high/low width		0.45	0.55	tCK(min)	
tKHKL	CLK rise or fall time		-	1.5	ns	
tCPH	CE# HIGH between subsequent burst operations		18	-	ns	
tCEM	CE# low pulse width	-40~85°C	-	8	µs	
tXPHS	Hybrid Sleep Exit CE# low pulse width		60	-	ns	
			-	tCEM	µs	
tCSP	CE# setup time to CLK rising edge		2.5	-	ns	
tCHD	CE# hold time from CLK falling edge		3	-	ns	
tCHD_HS	CE# hold time from CLK rising edge for Hybrid Sleep Entry command		6	-	ns	
tSP	Setup time to active CLK edge		2		ns	
tHD	Hold time from active CLK edge		2		ns	
tHZ	Chip disable to DQ output high-Z			5.5	ns	
tACLK	Clock to output delay		2	5.5	ns	
tKOH	Data hold time from clock falling edge		1.5	-	ns	
tHS	Minimum Hybrid Sleep duration		150	-	µs	
tXHS	Hybrid Sleep Exit CE# low to CLK setup time		150	-	µs	
tRST	Time between end of RST CMD to next valid CMD		50		ns	

Chiplus reserves the right to change product or specification without notice.

Package Outline

8L SOP-150mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	B	C	e	D	H	E	L	h	θ
mm	Min.	1.35	0.10	0.33	0.19	1.27 BSC	4.80	5.80	3.80	0.40	0.25	0
	Nom.	--	--	--	--		--	--	--	--	--	--
	Max.	1.75	0.25	0.51	0.25		5.00	6.20	4.00	1.27	0.50	8
inch	Min.	0.0532	0.0040	0.013	0.0075	0.050 BSC	0.1890	0.2284	0.1497	0.016	0.0099	0
	Nom.	--	--	--	--		--	--	--	--	--	--
	Max.	0.0688	0.0098	0.020	0.0098		0.1988	0.2440	0.1574	0.050	0.0196	8

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